

FIG. 2

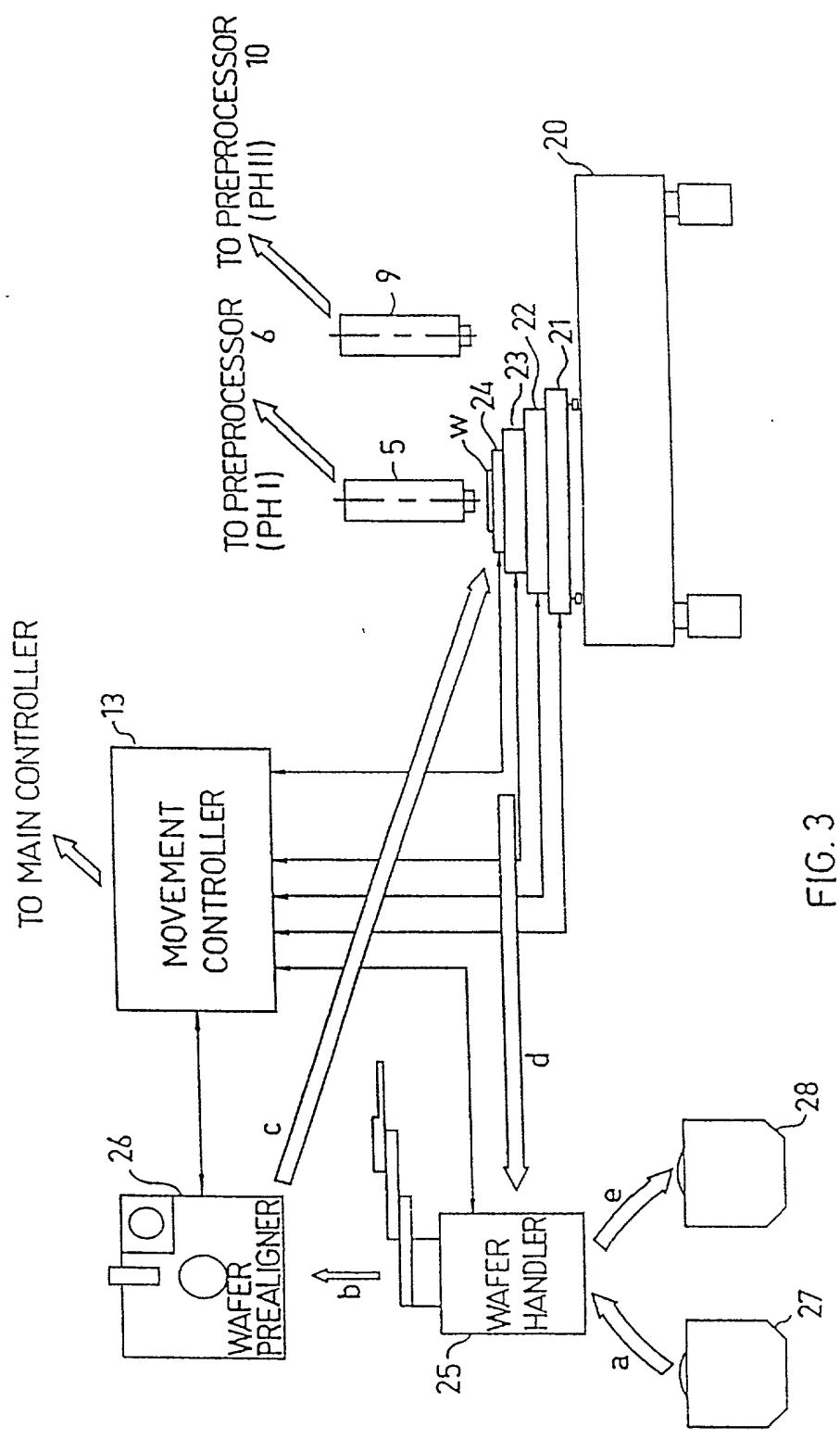


FIG. 5

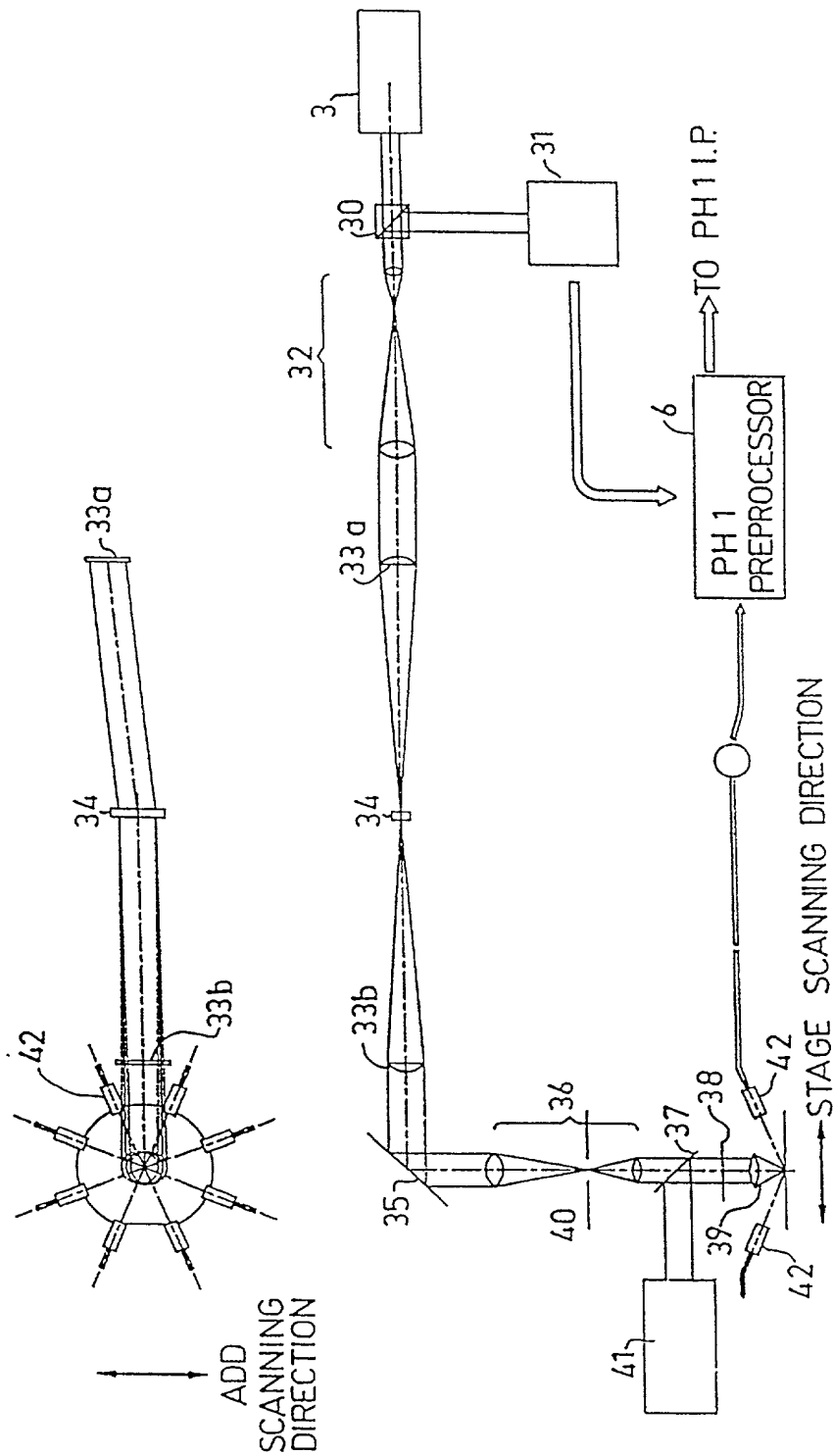


FIG. 4

FIG. 6

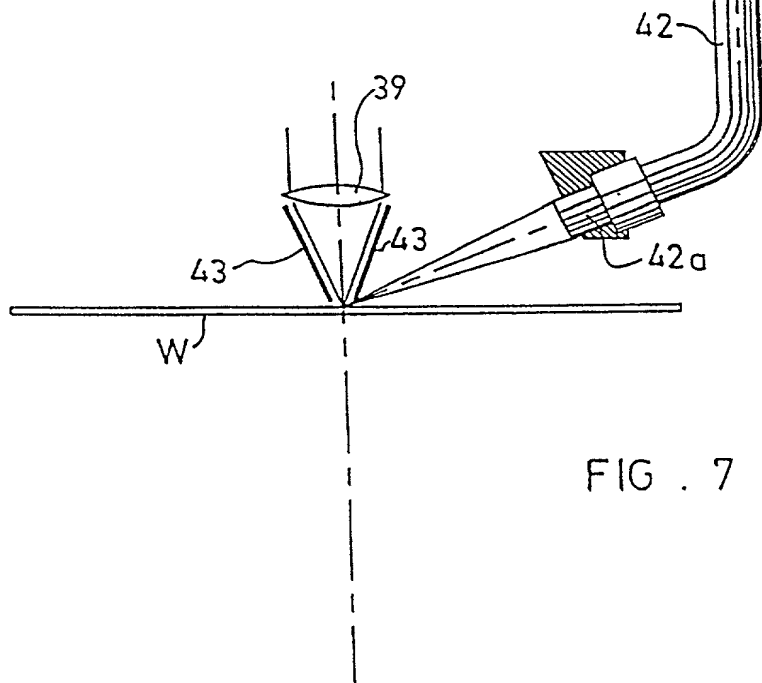
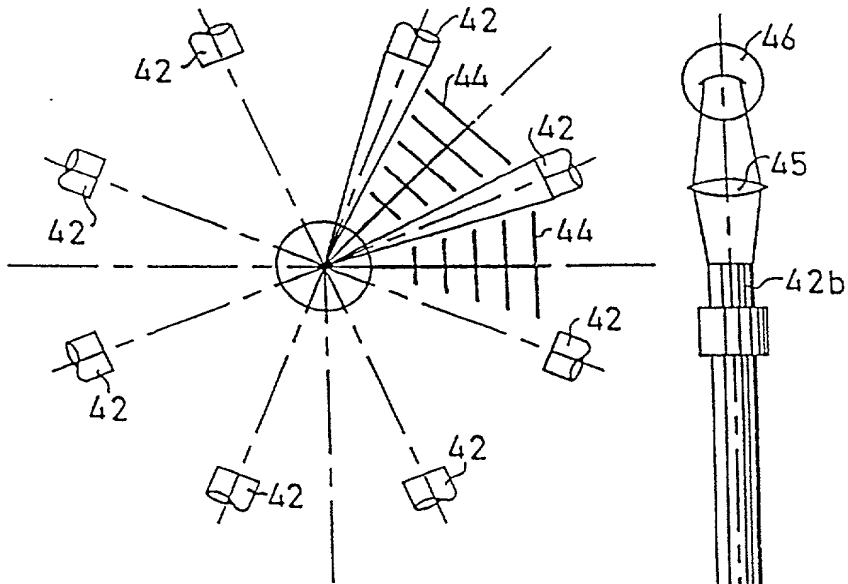


FIG. 7

FIG. 6a

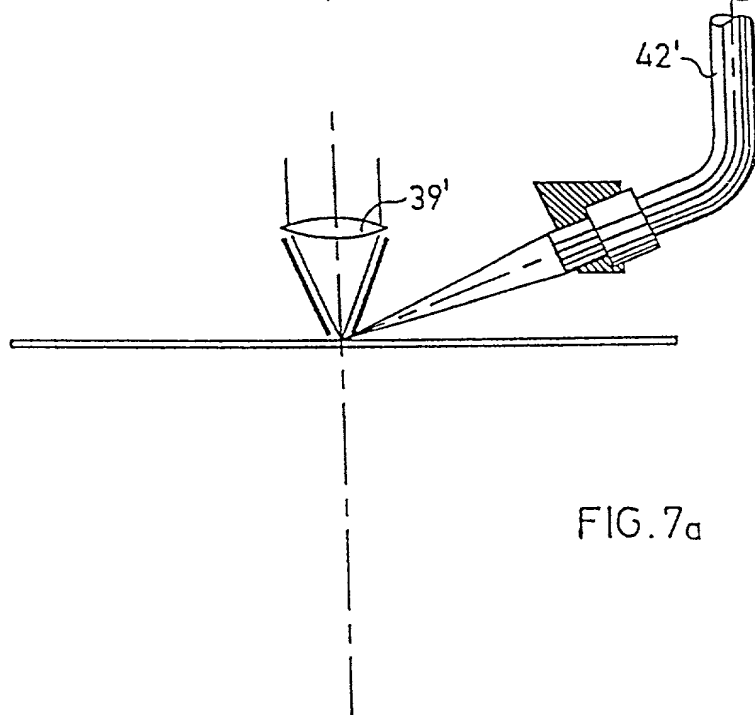
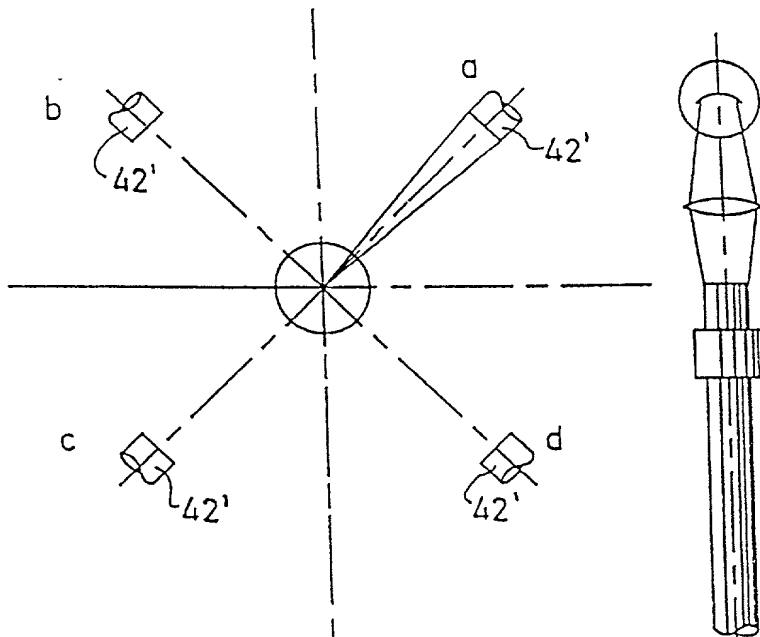


FIG. 7a

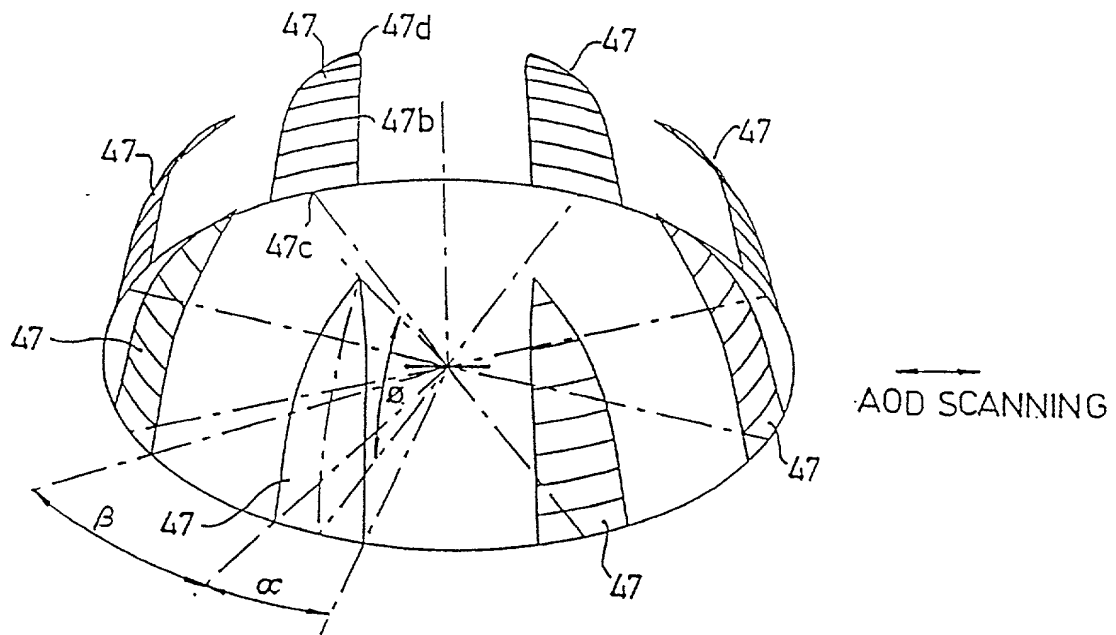


FIG 8

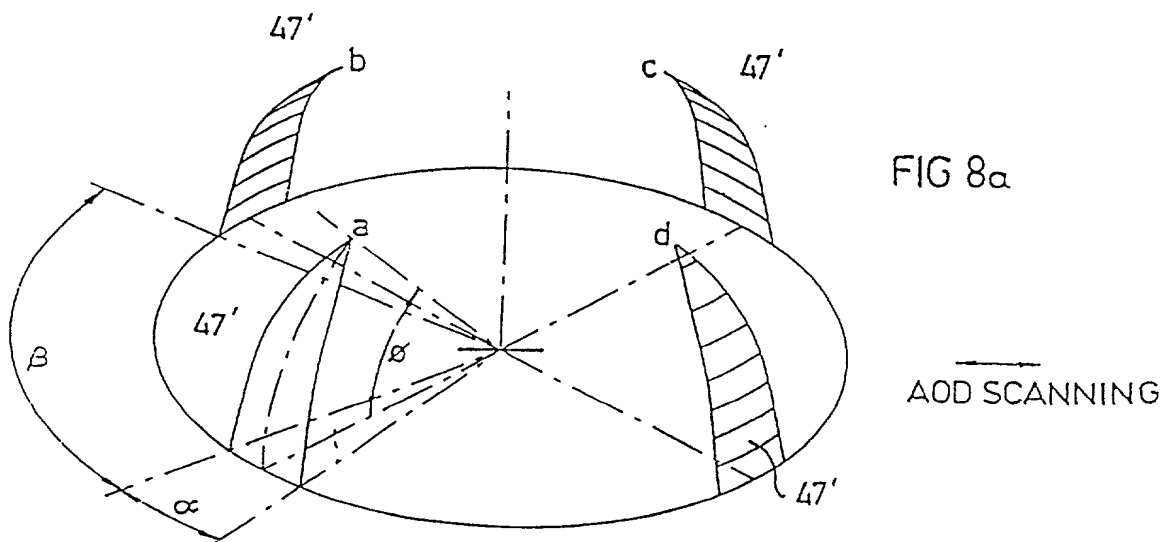


FIG 8a

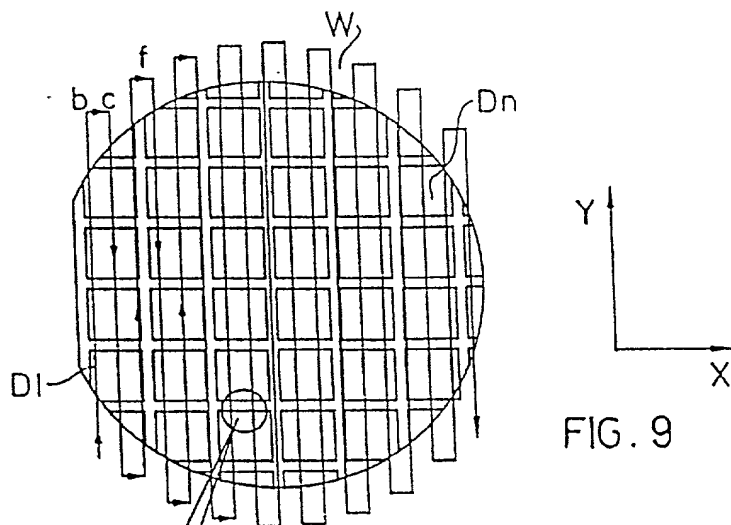


FIG. 9

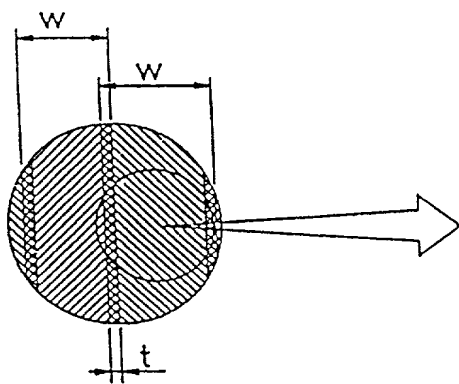


FIG. 10

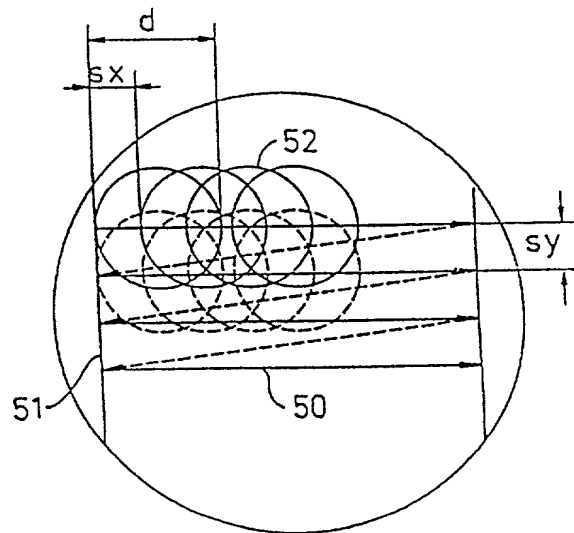
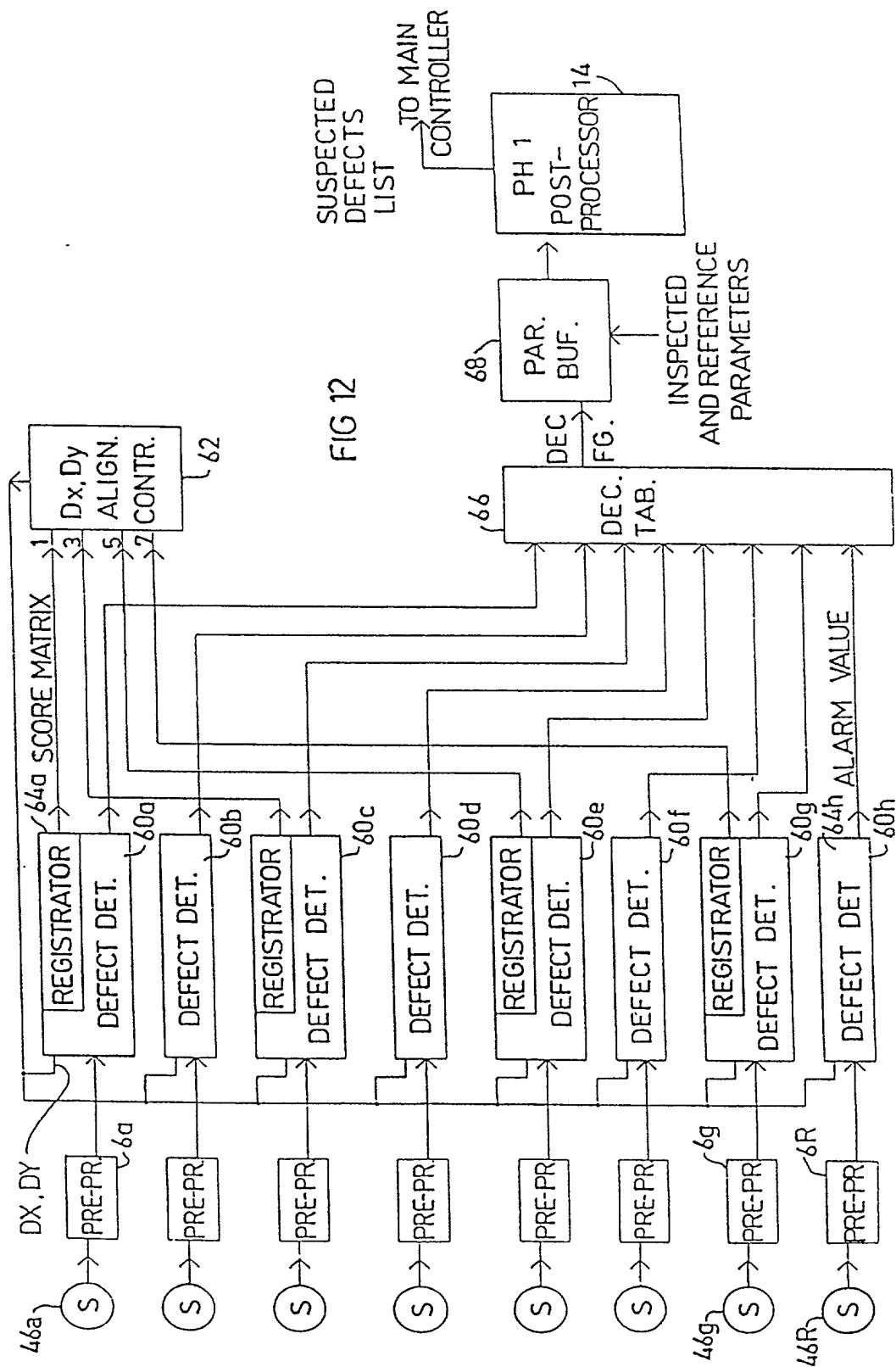


FIG. 11





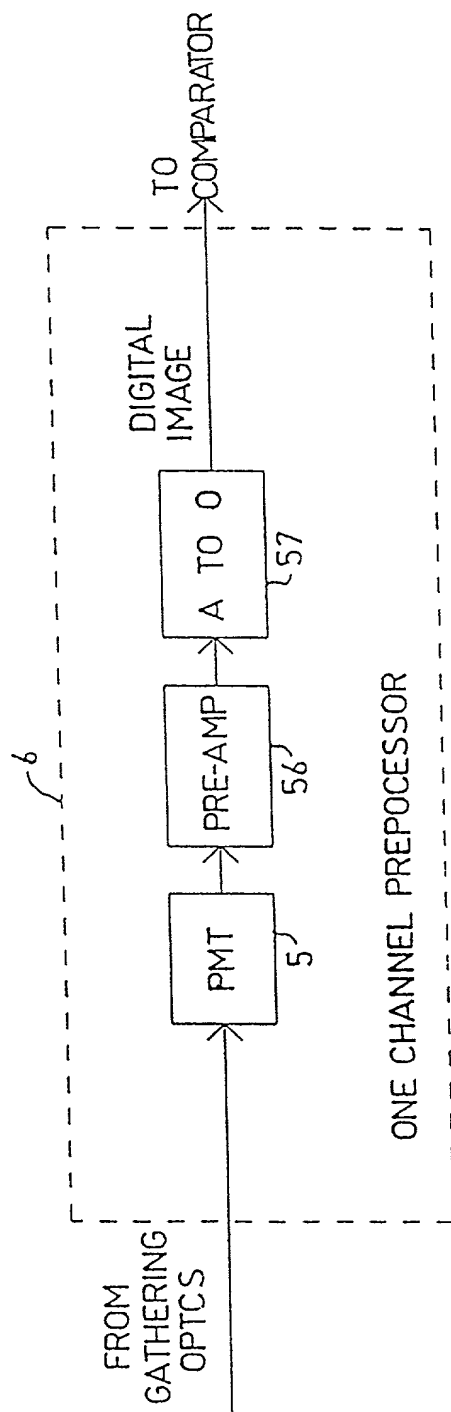


FIG. 13

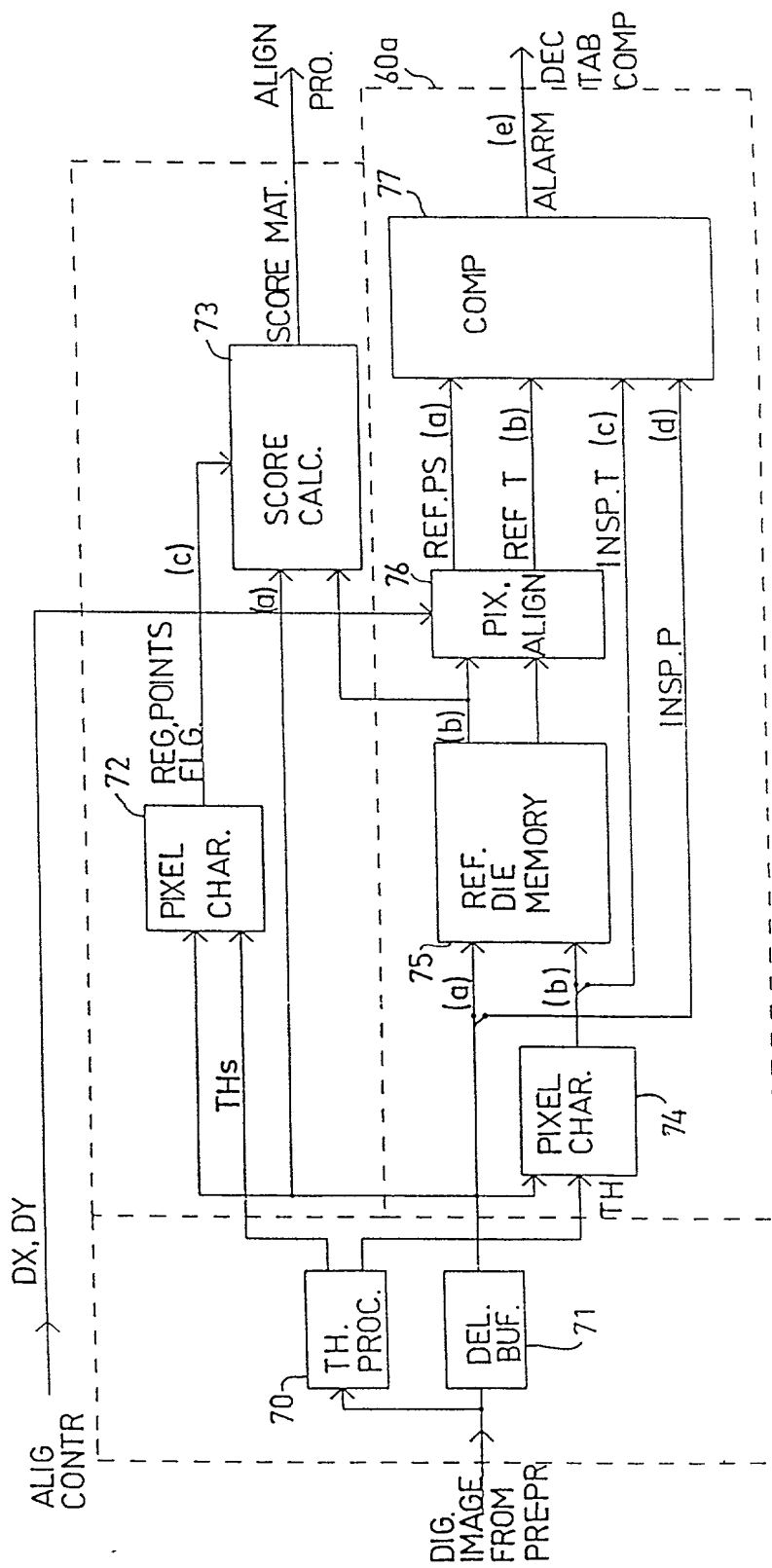


FIG. 14

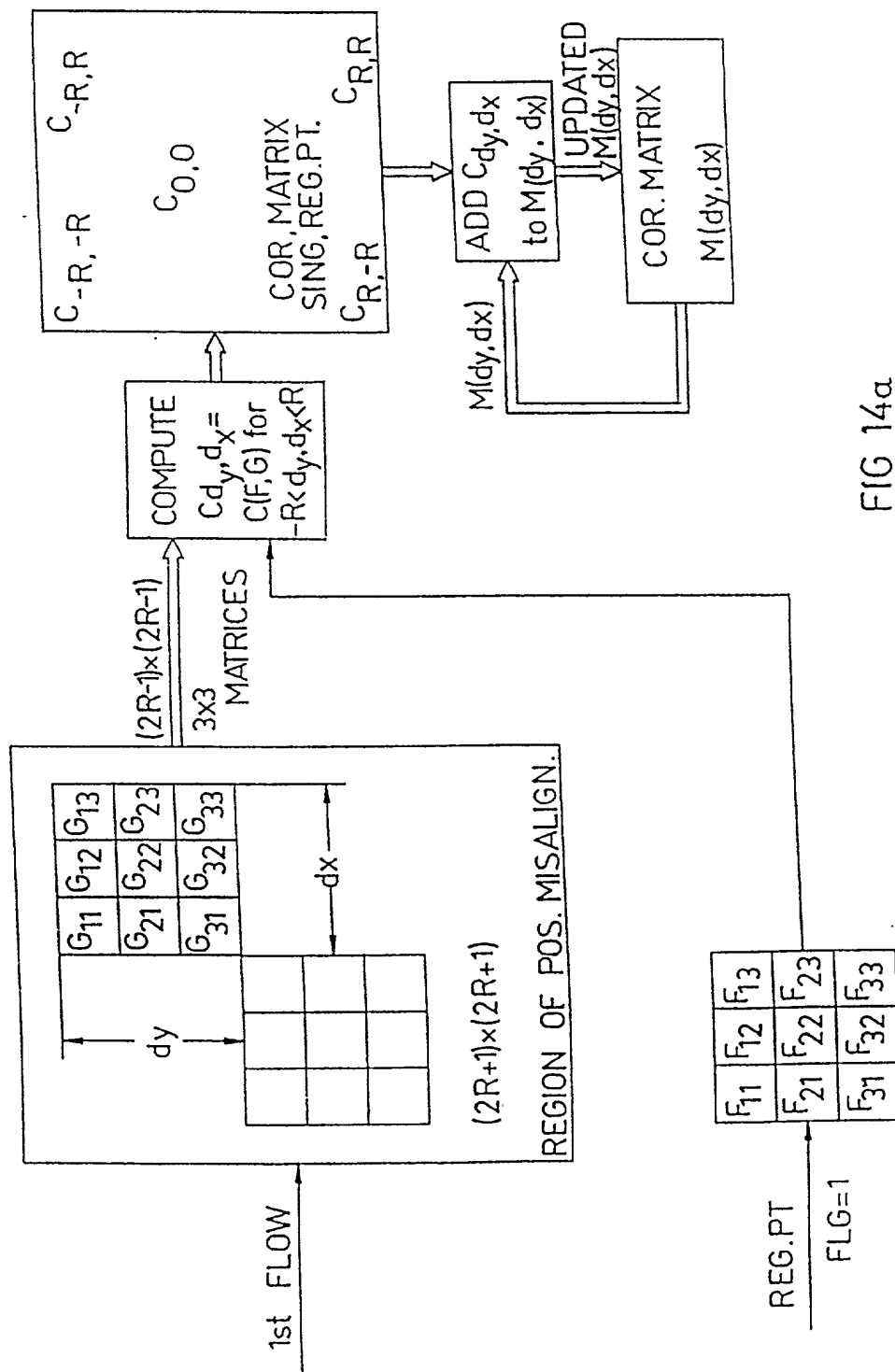


FIG 14a

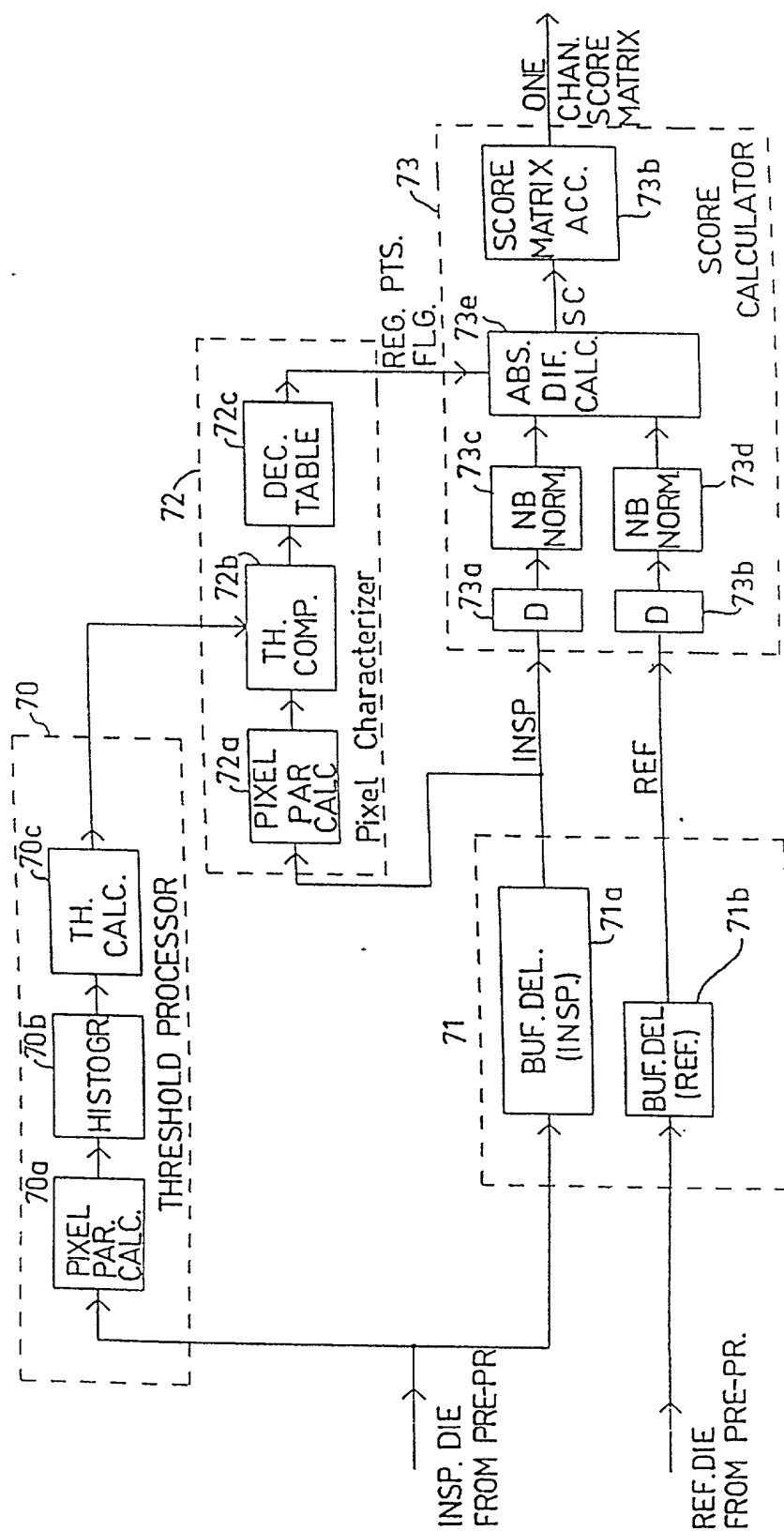


FIG. 15

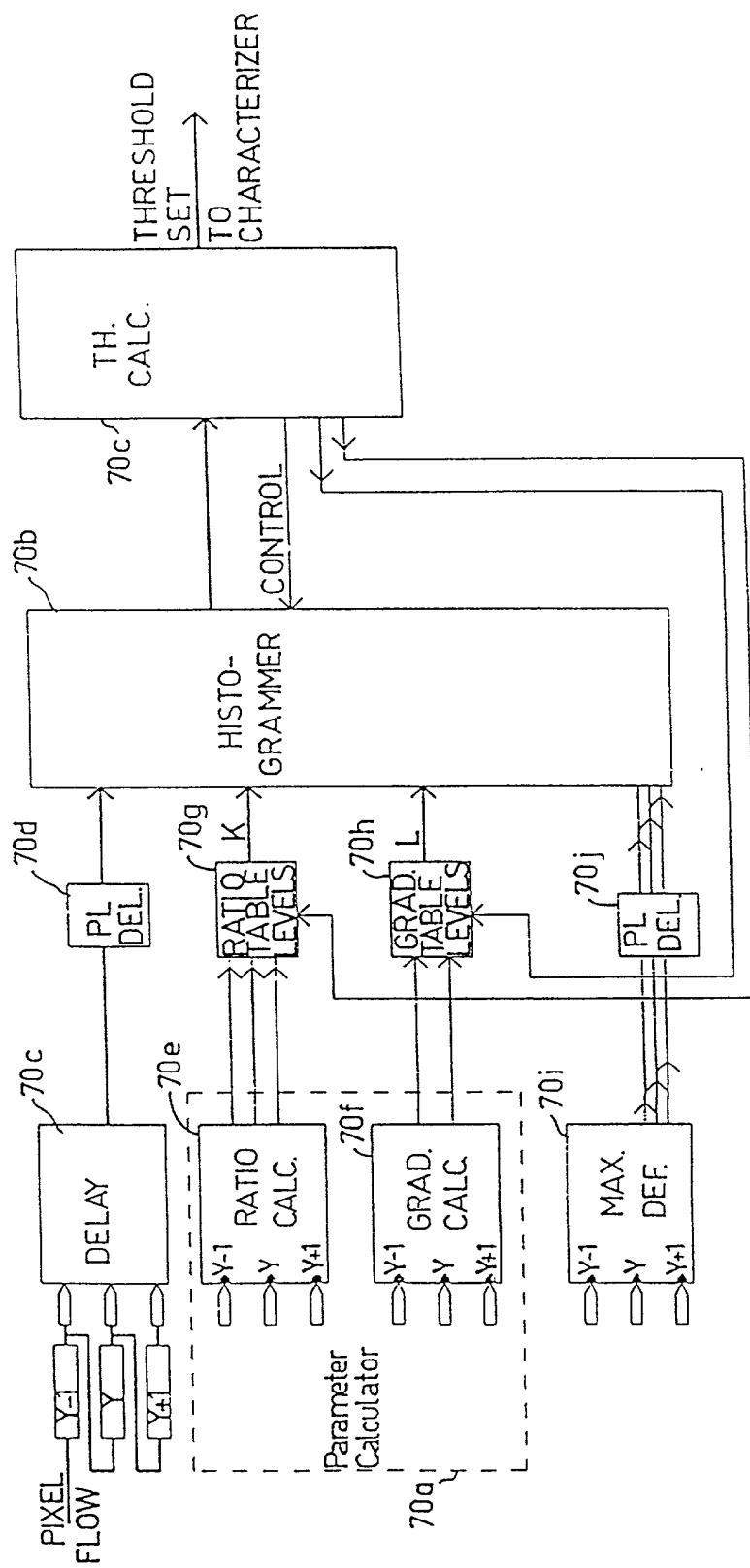
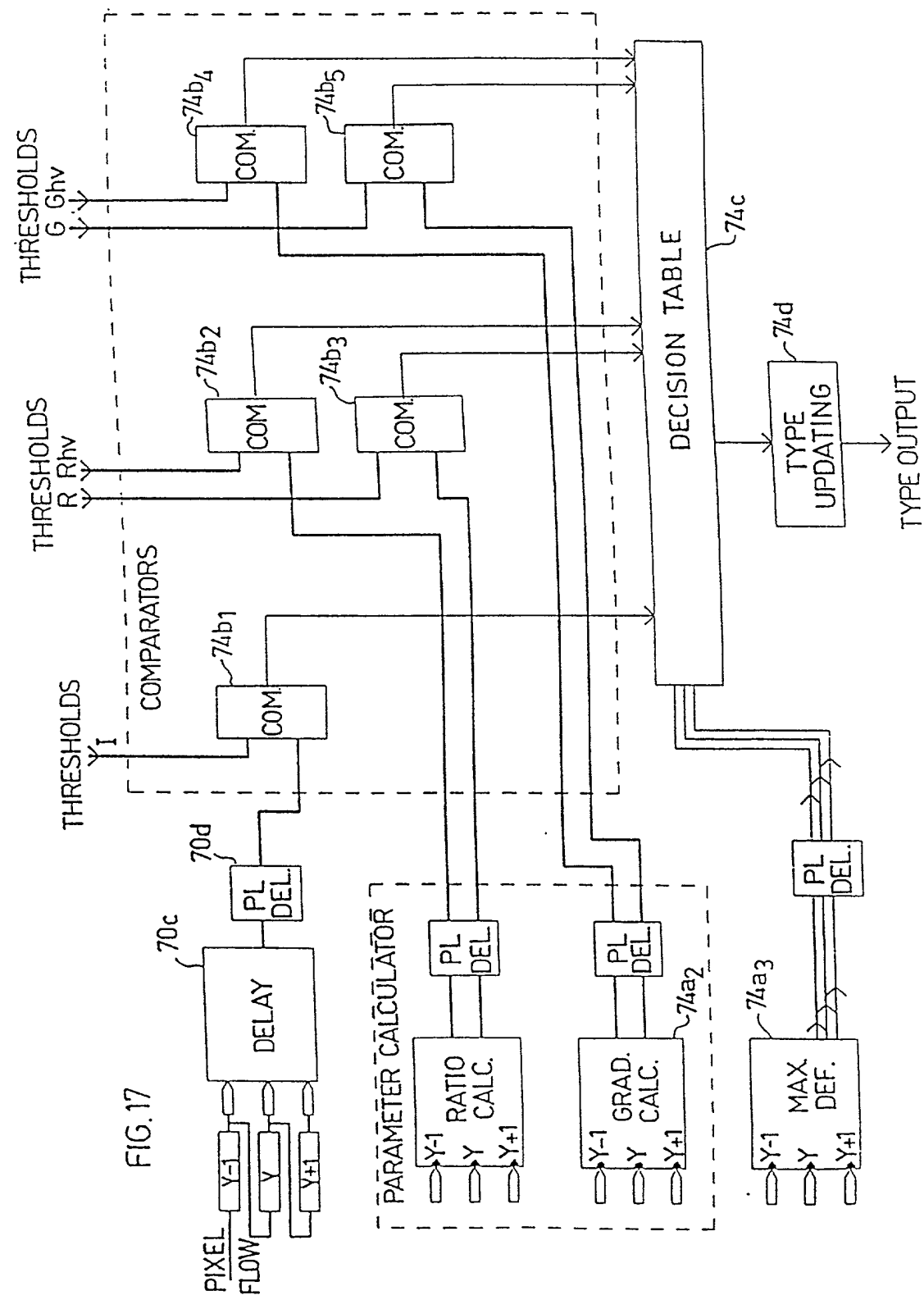
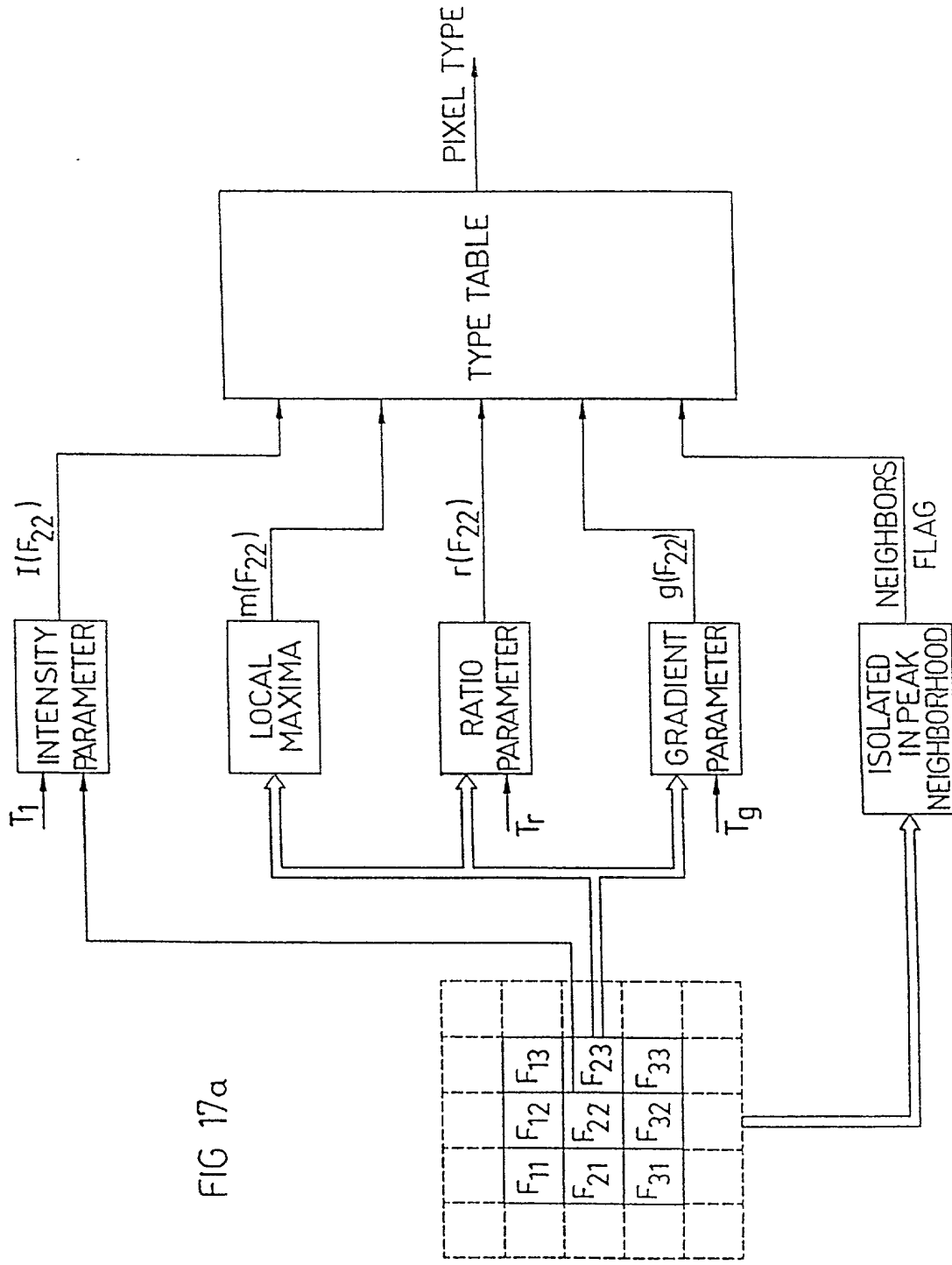


FIG. 16

FIG. 17







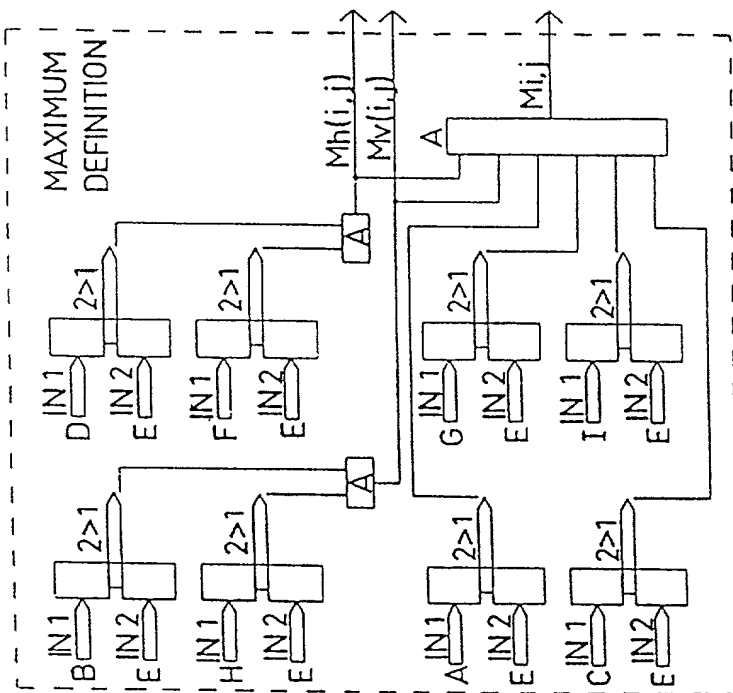


FIG 20

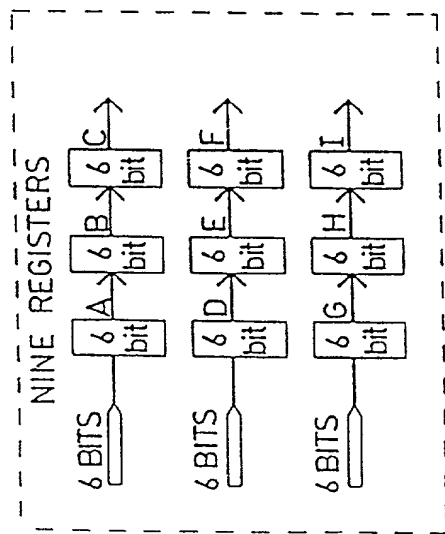


FIG 21a

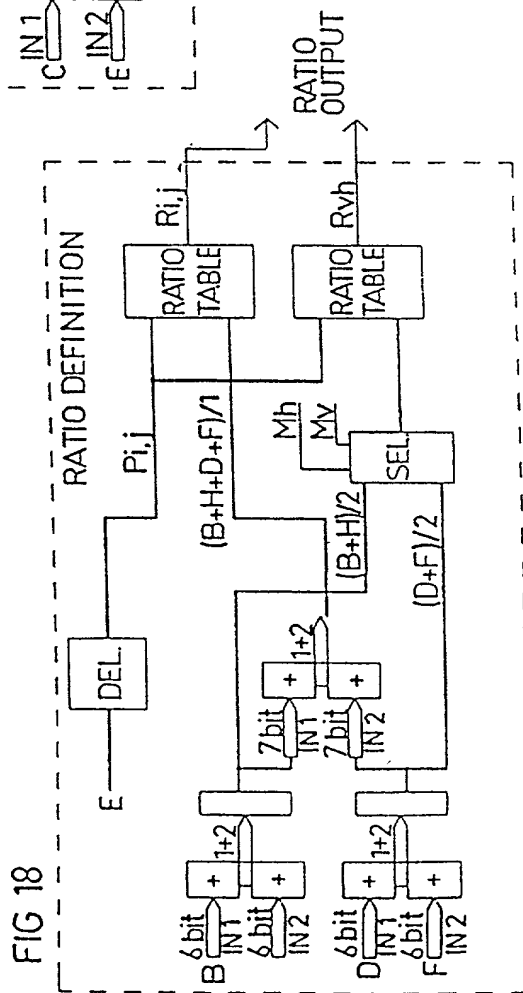
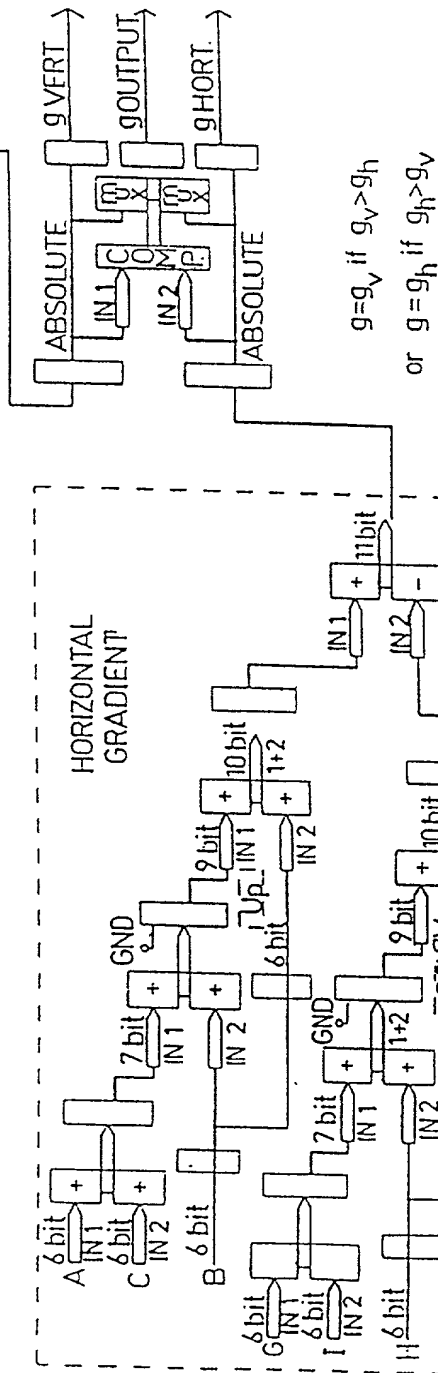
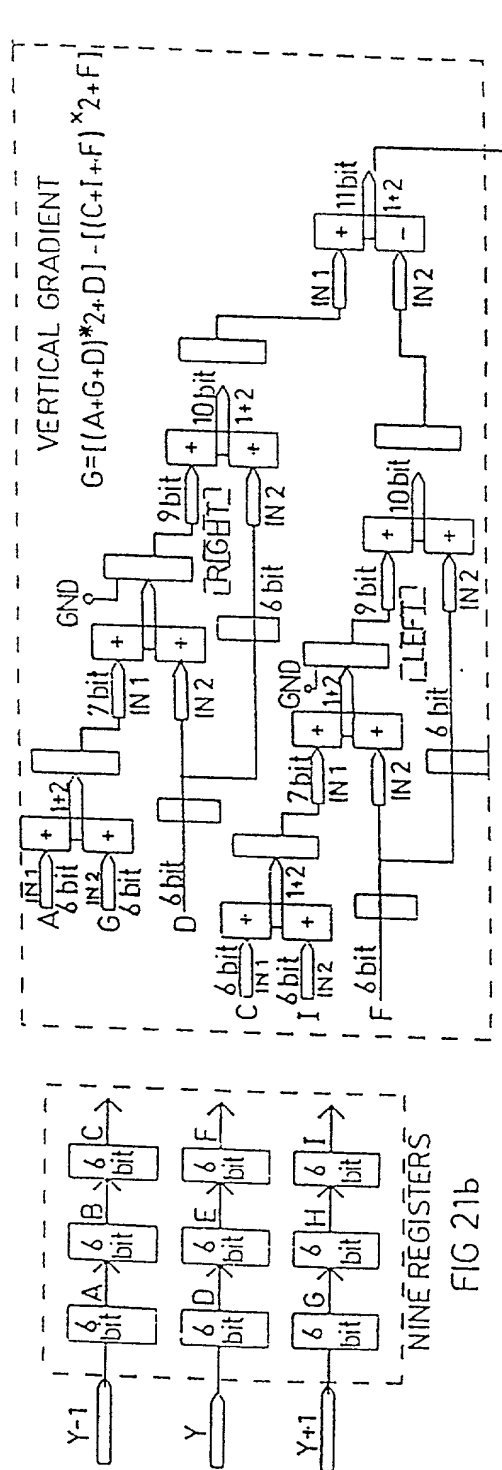
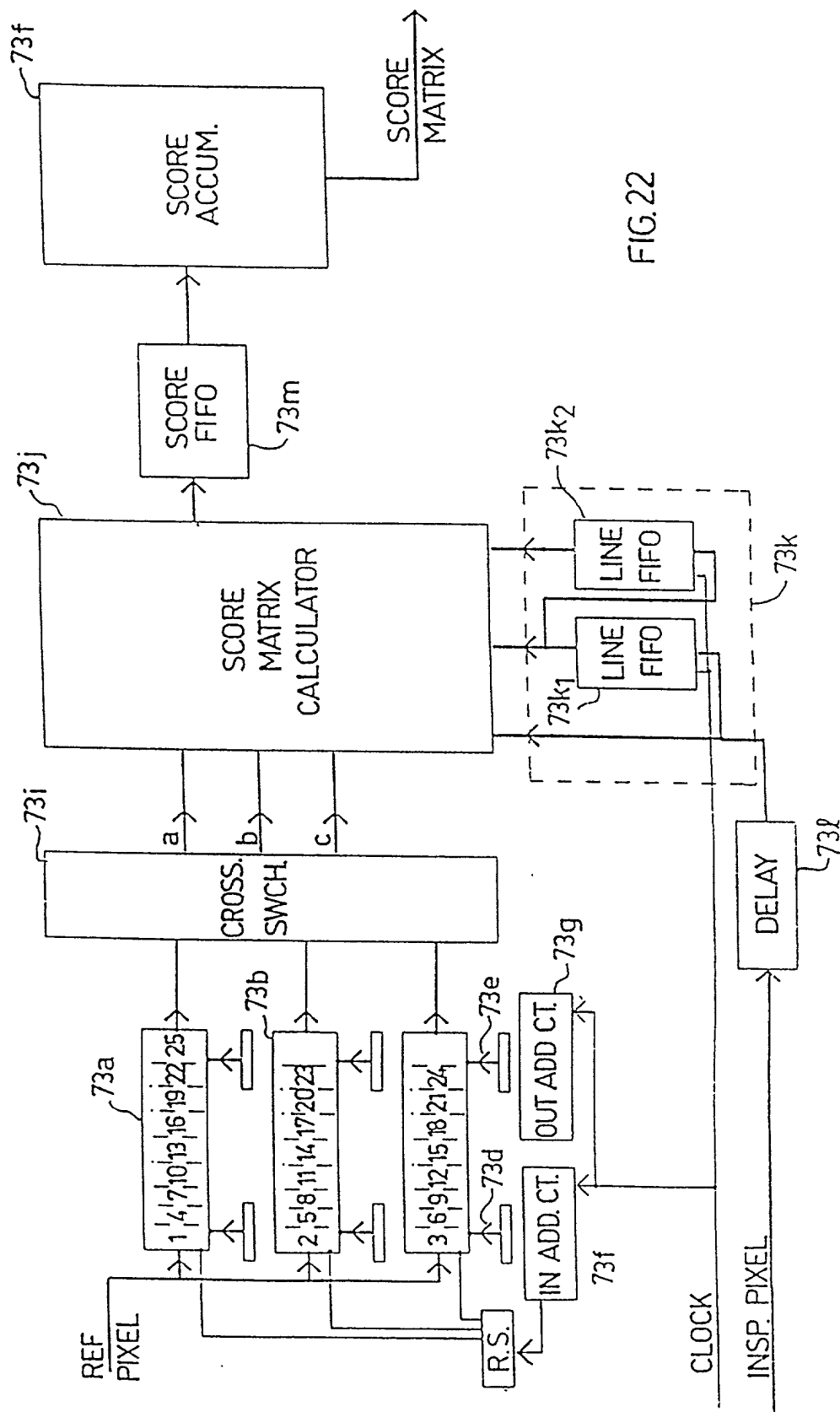


FIG 18





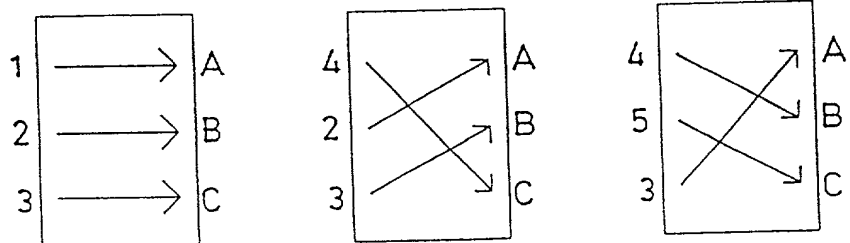


FIG . 22a

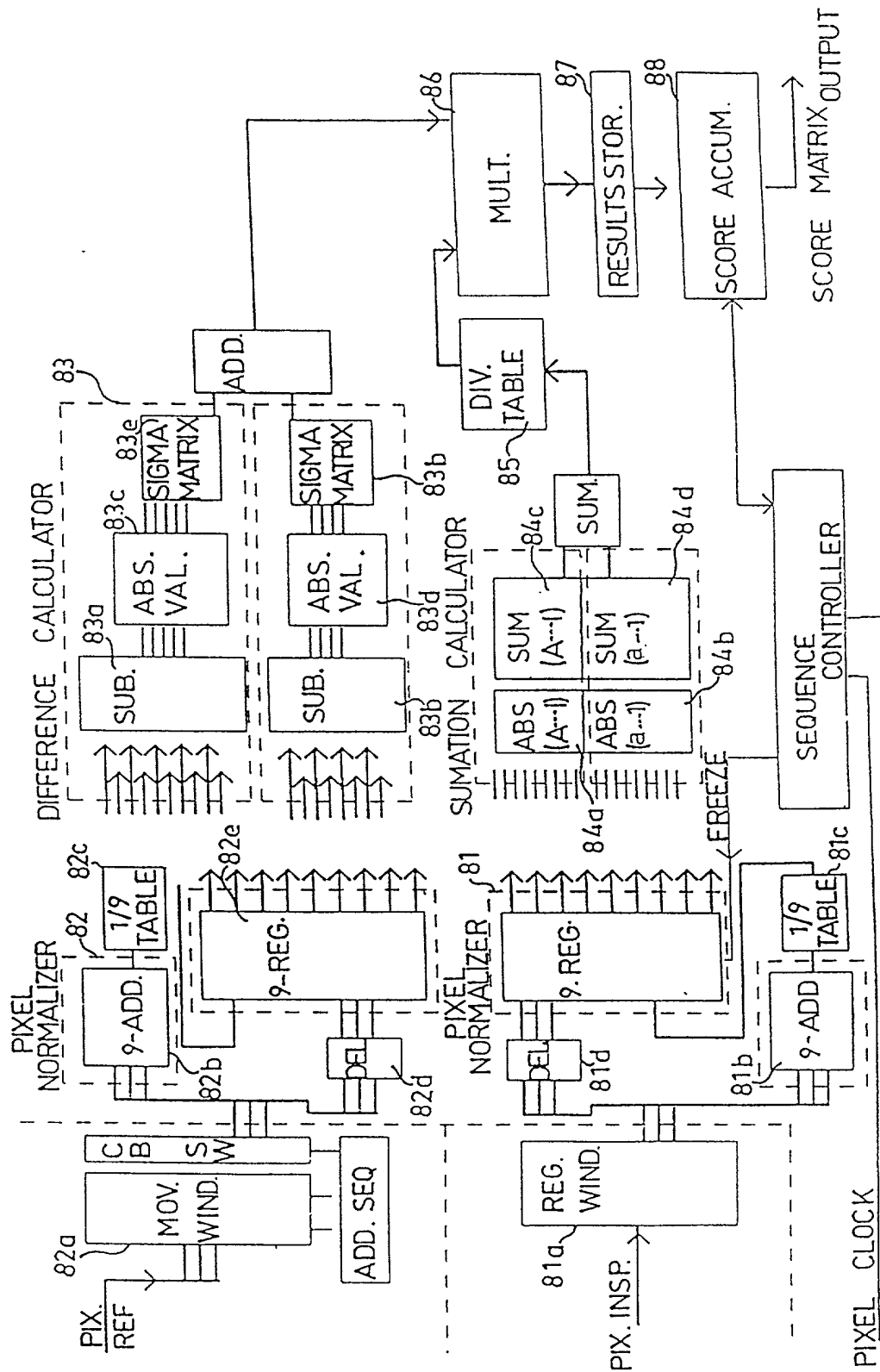
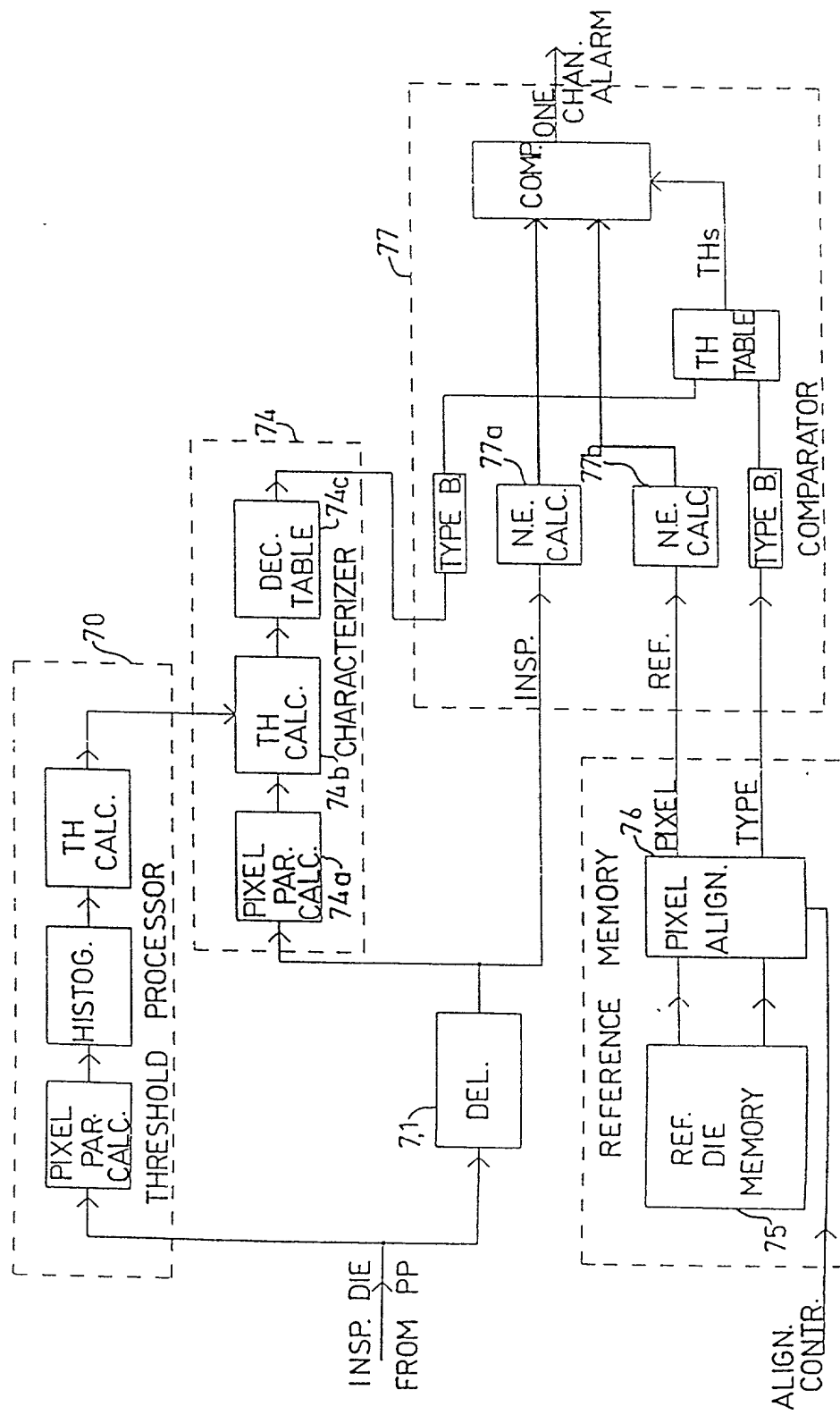


FIG. 23



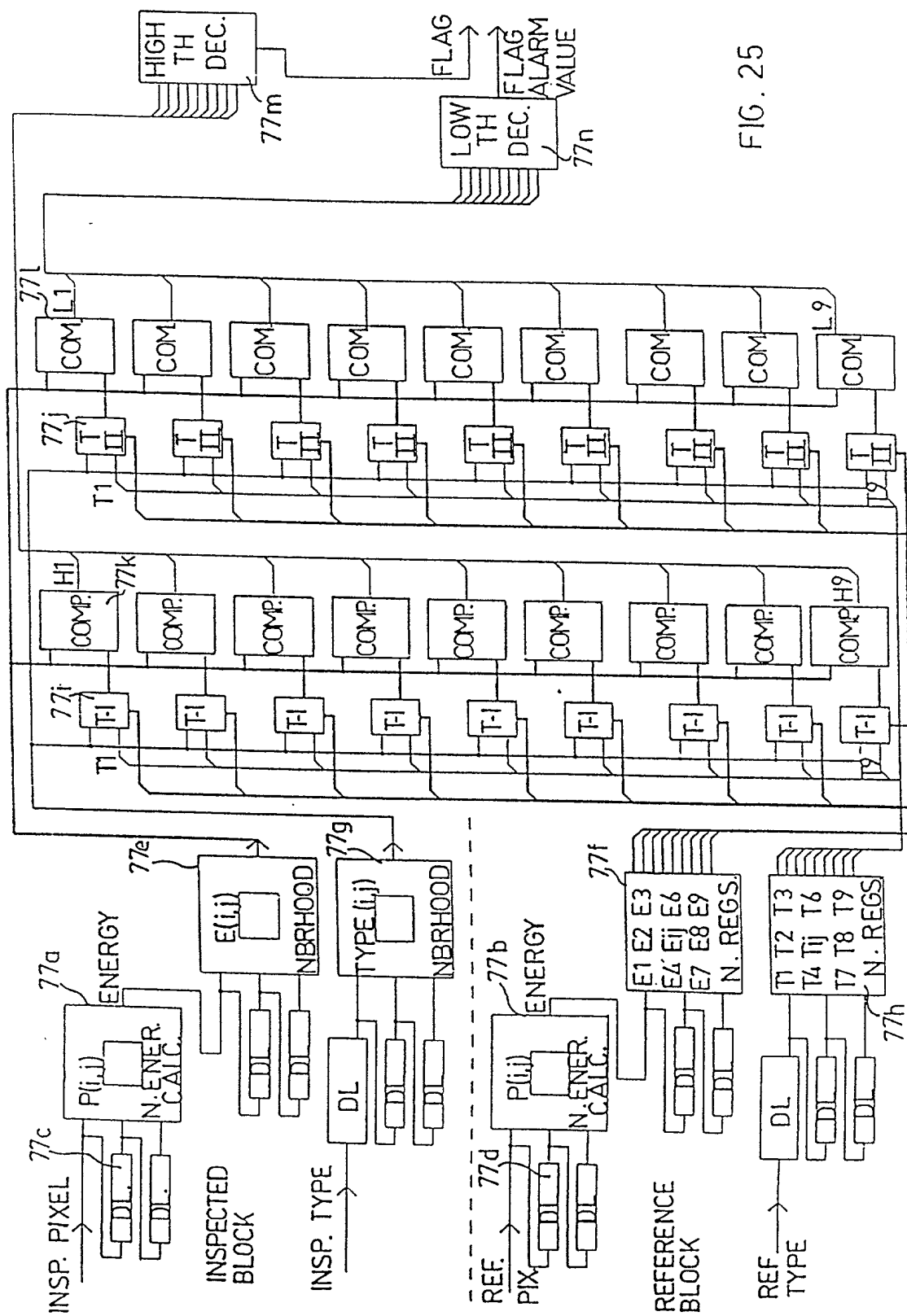


FIG. 25

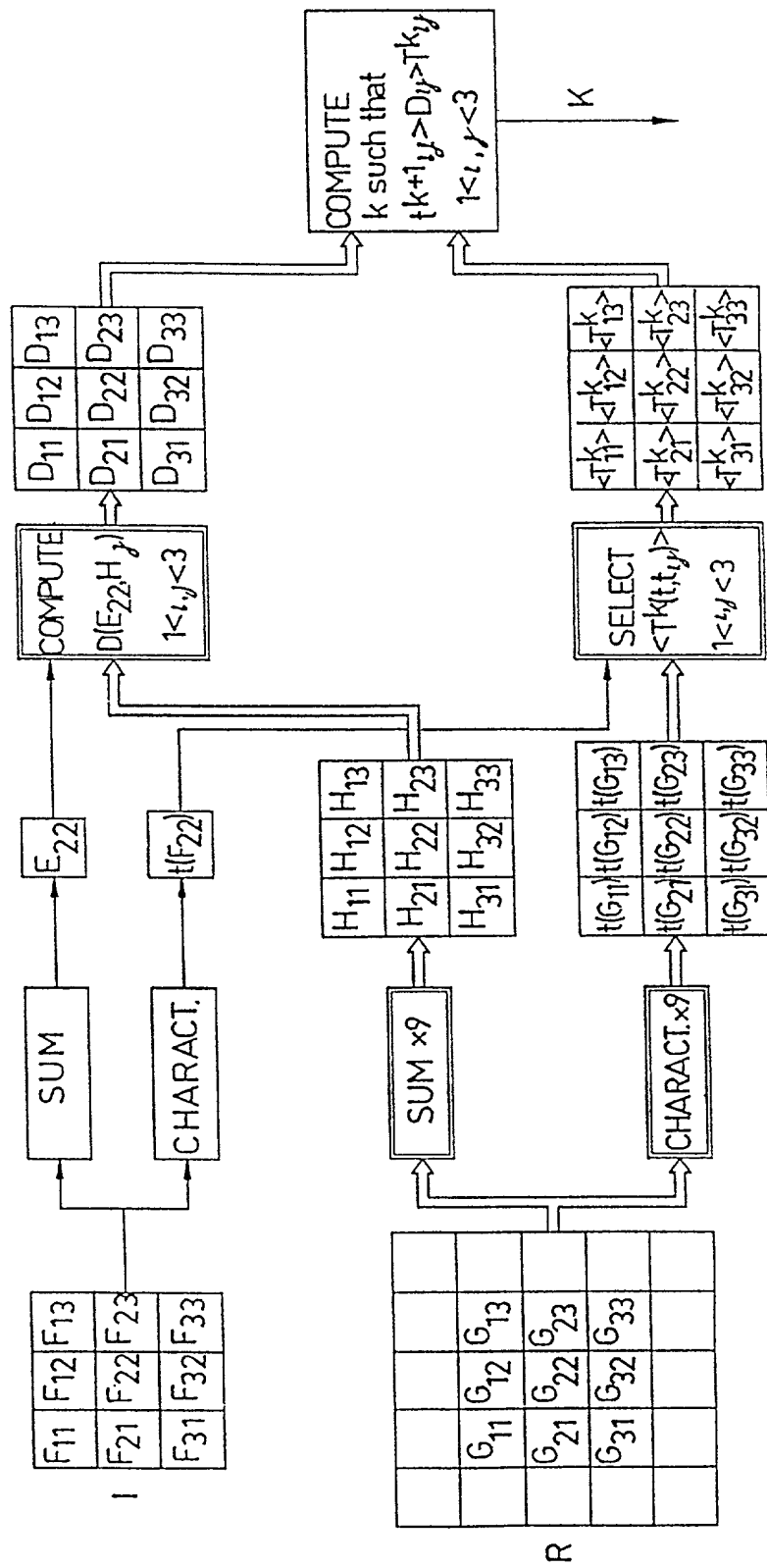


FIG 25a



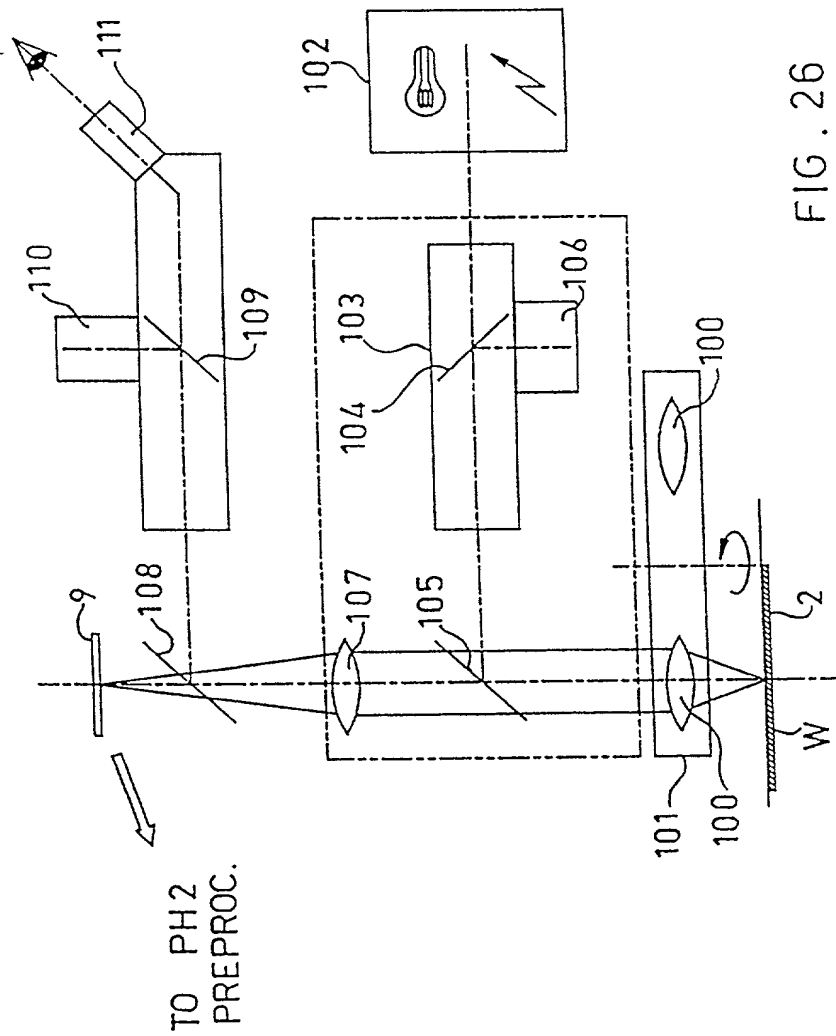


FIG. 26

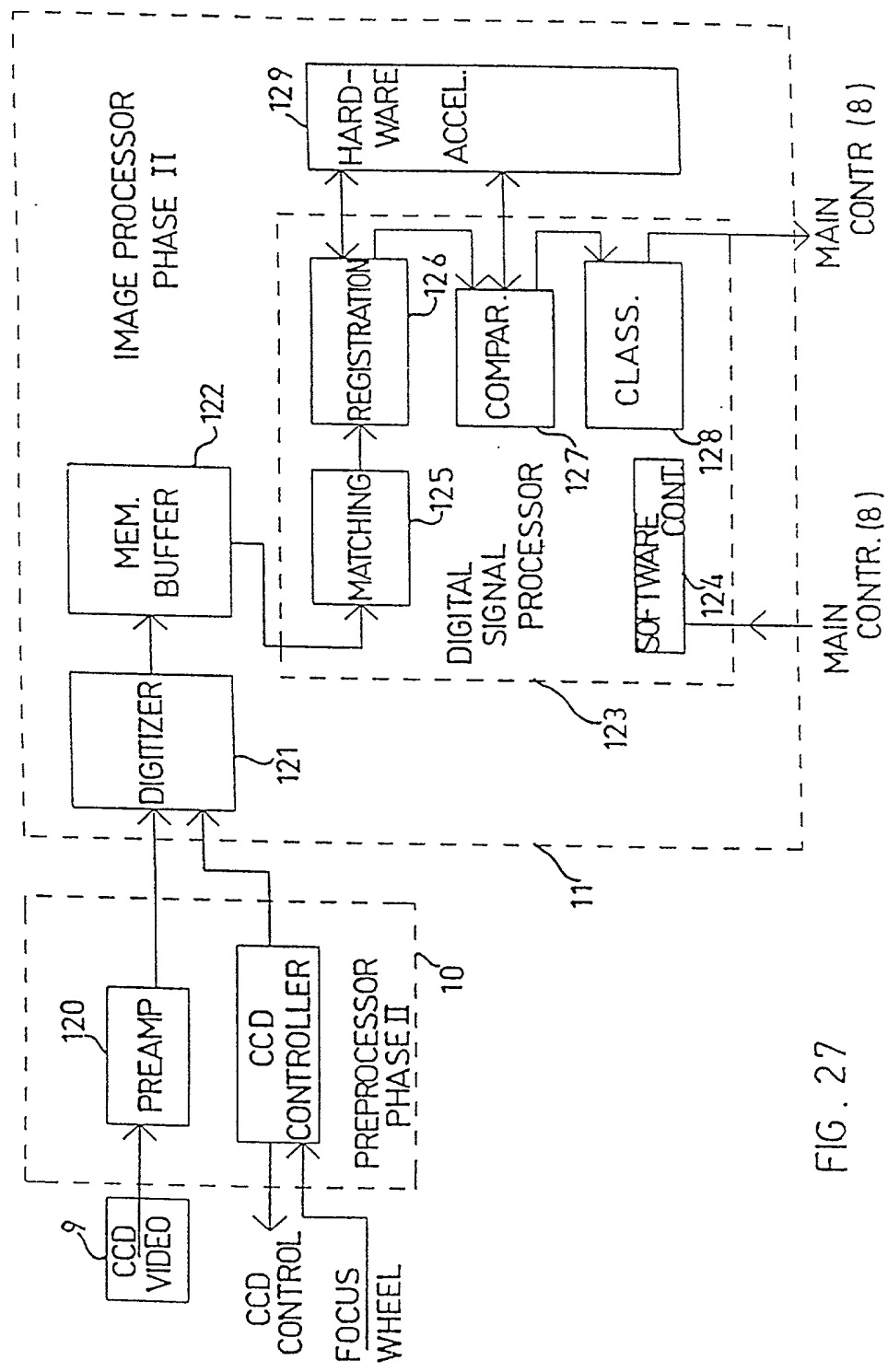


FIG. 27

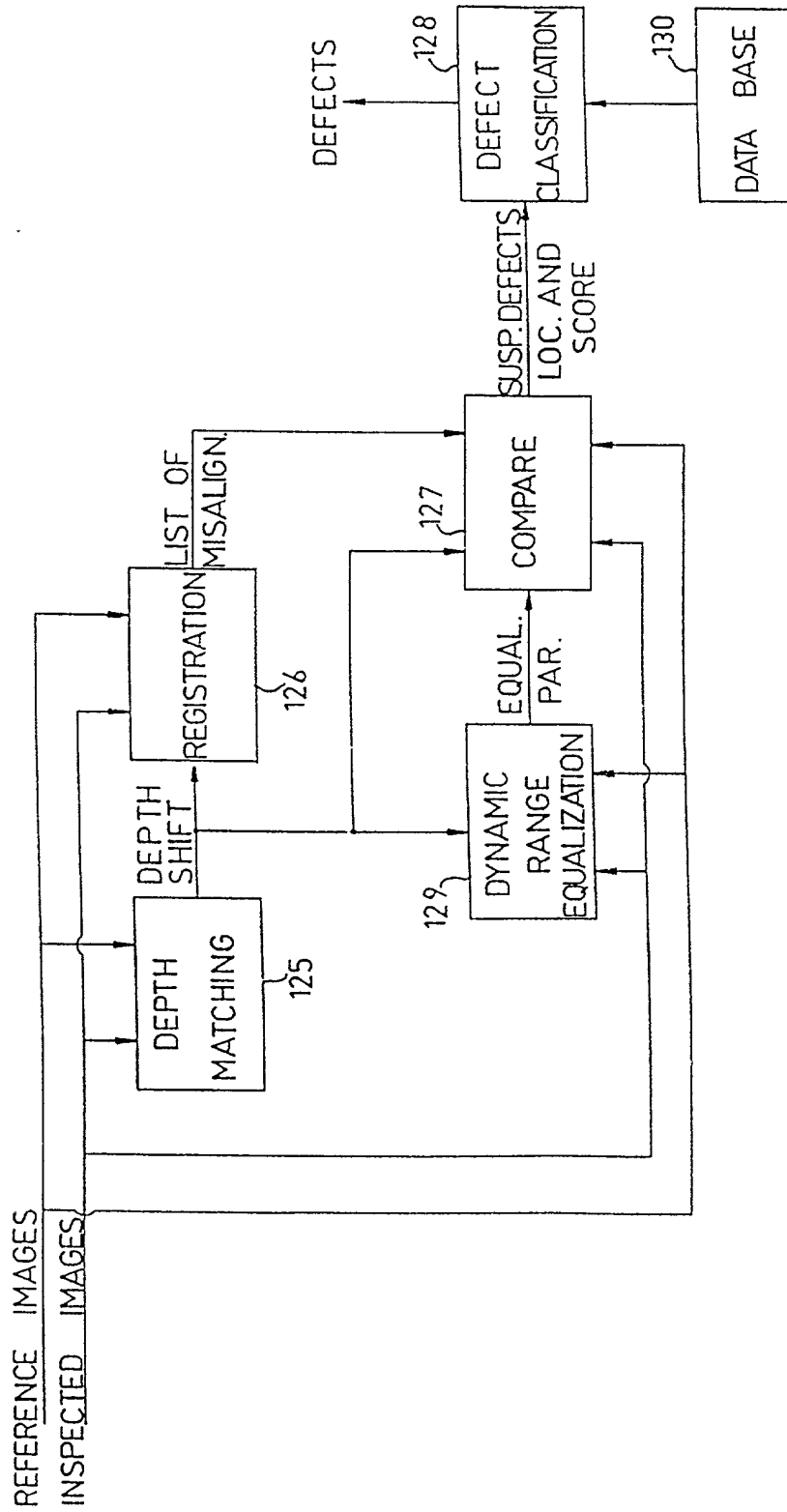


FIG. 28

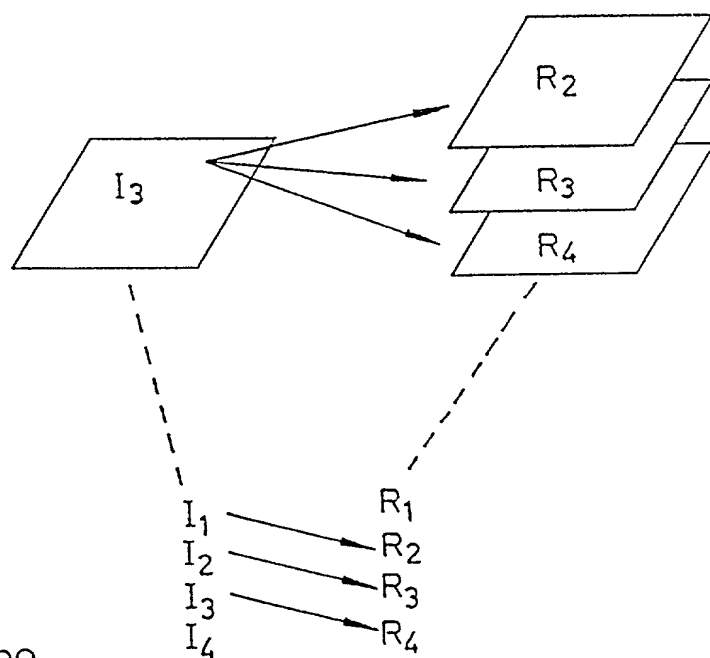


FIG. 29

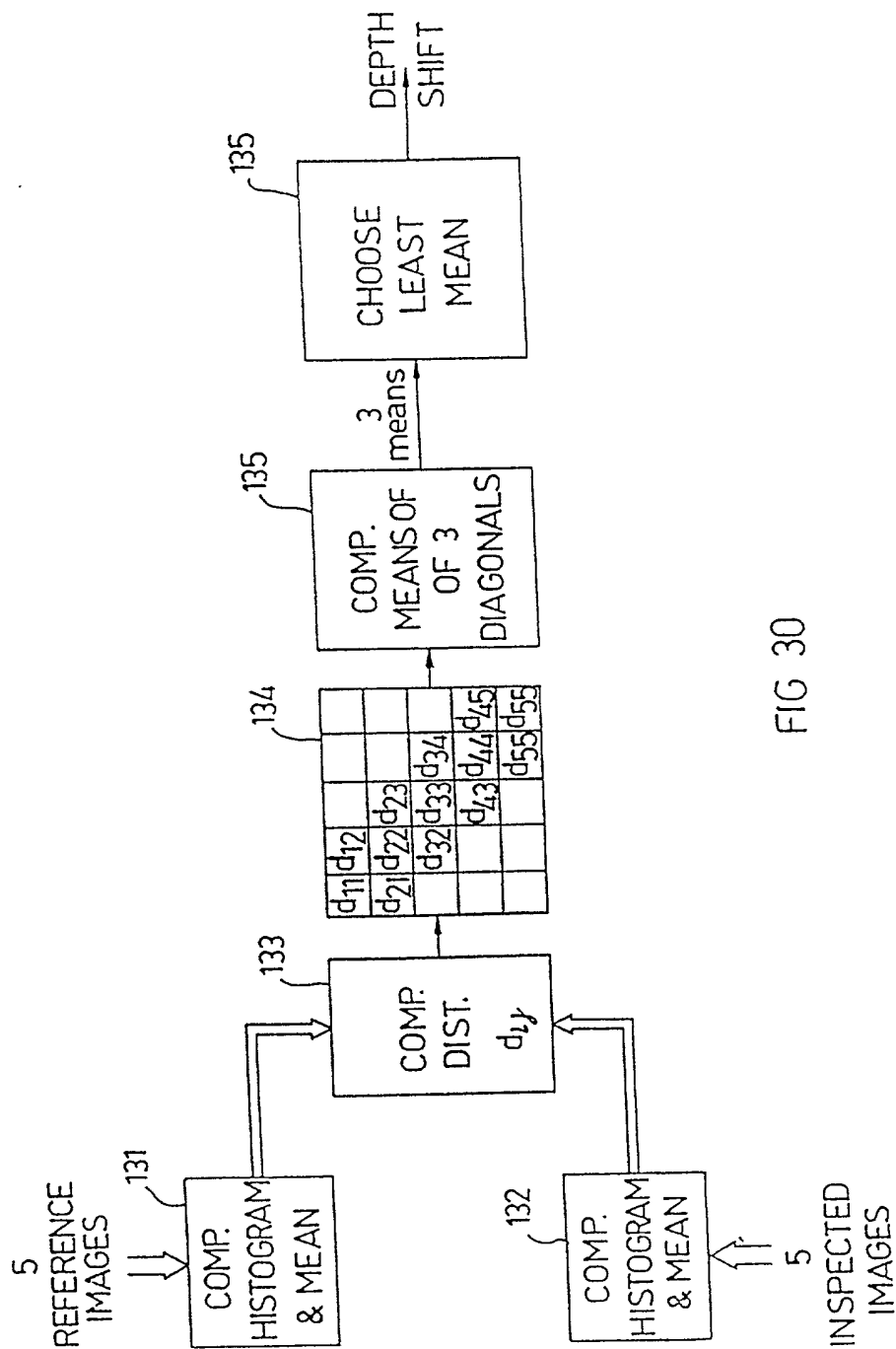


FIG 30

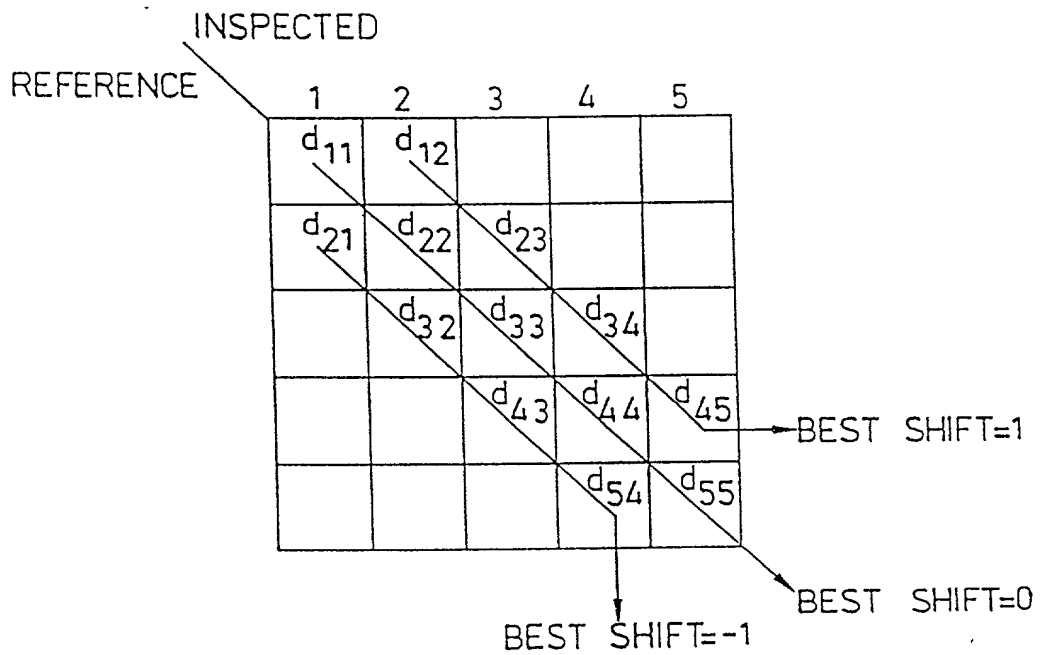


FIG . 31

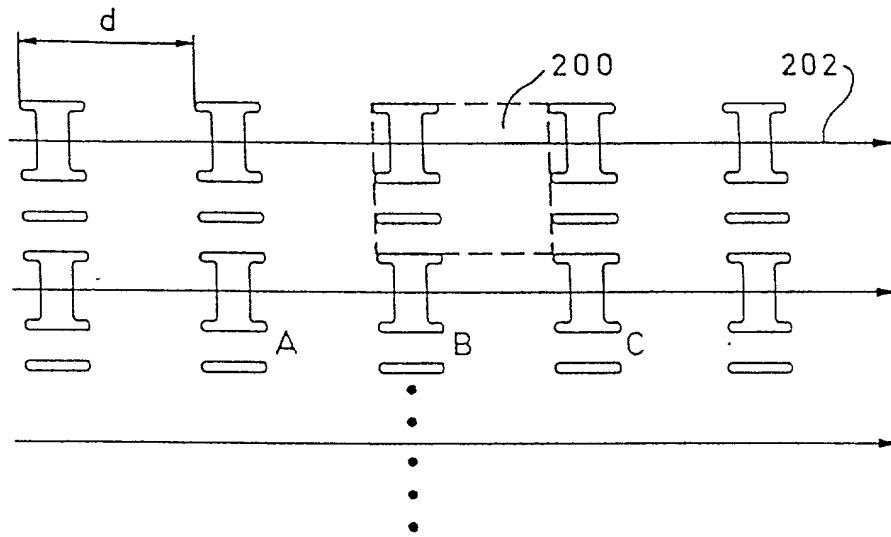


FIG. 32

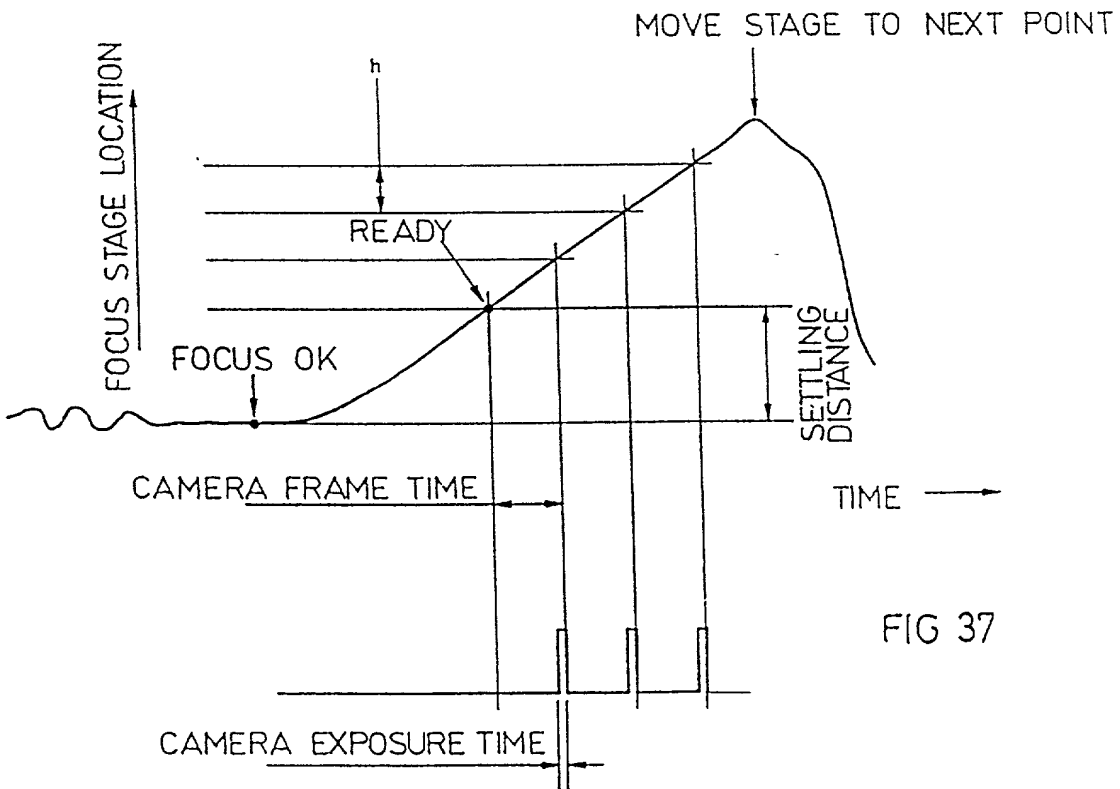
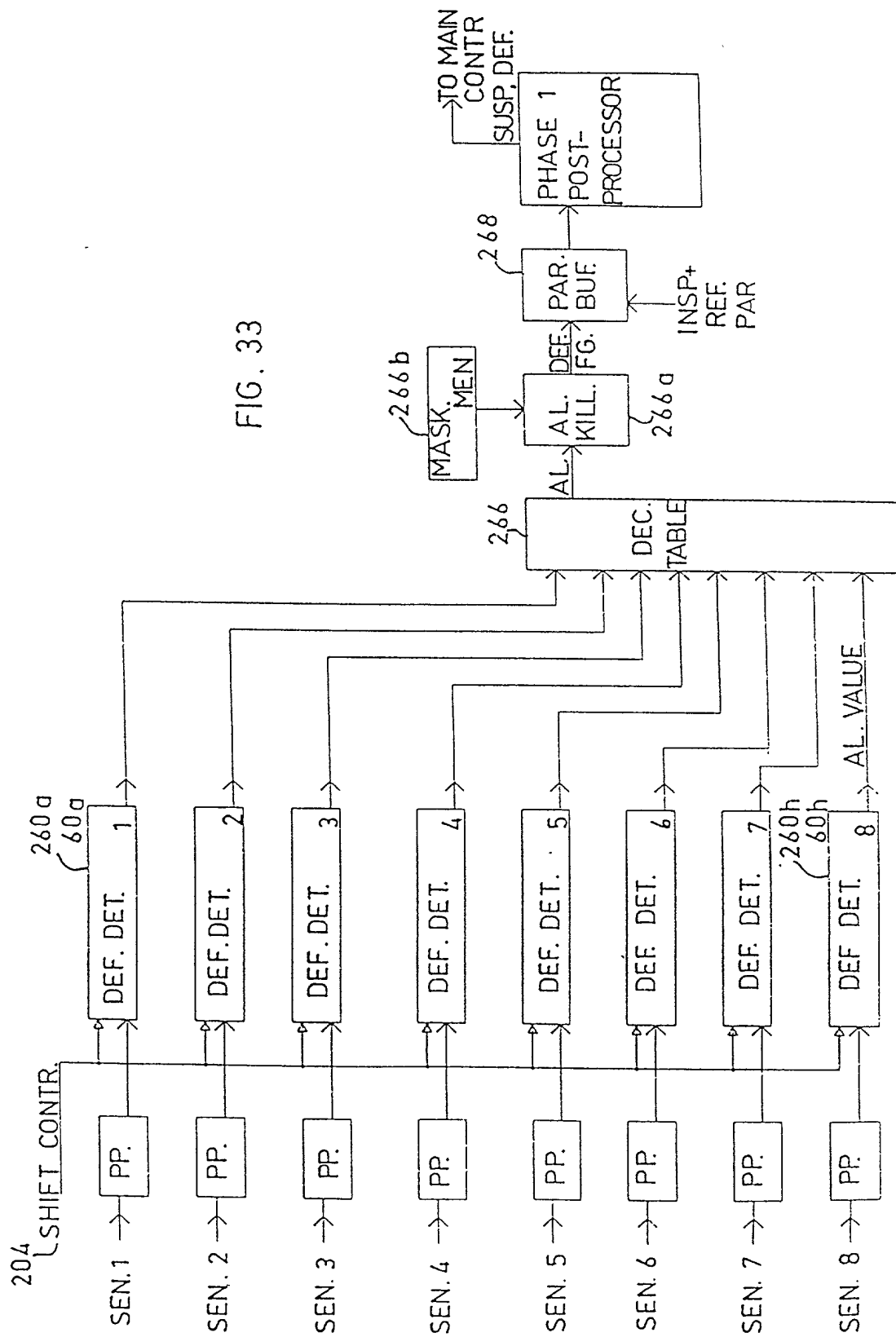
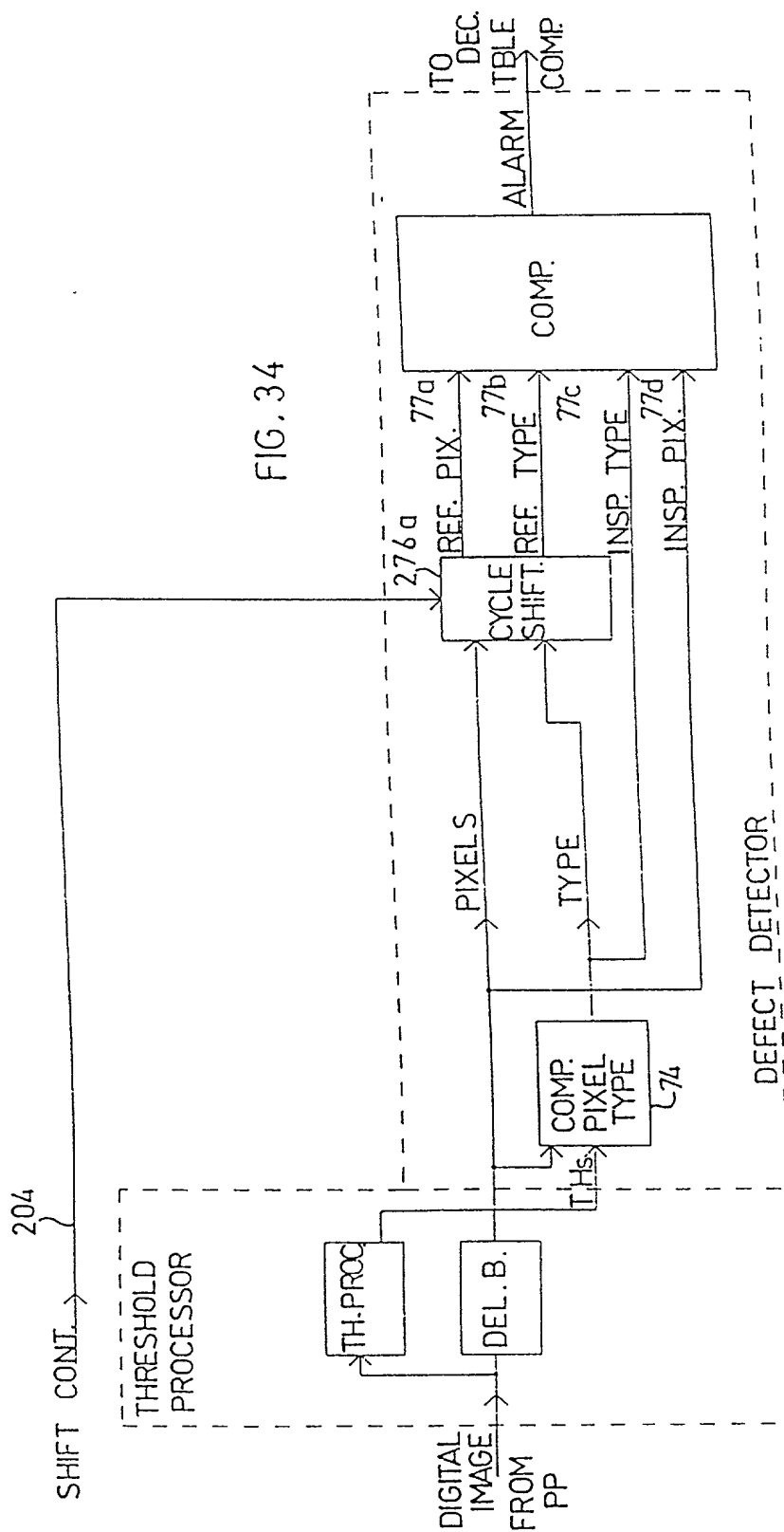
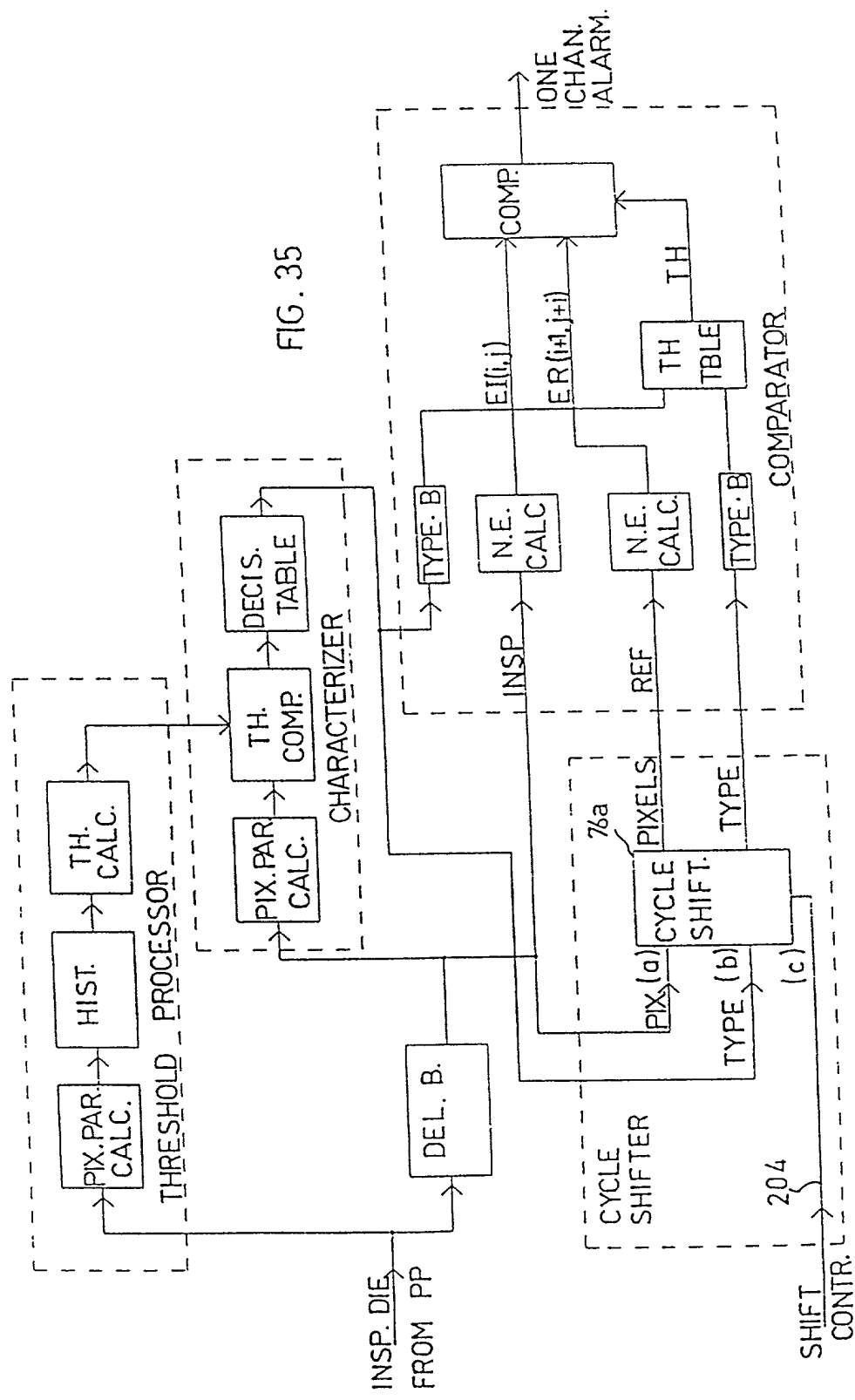


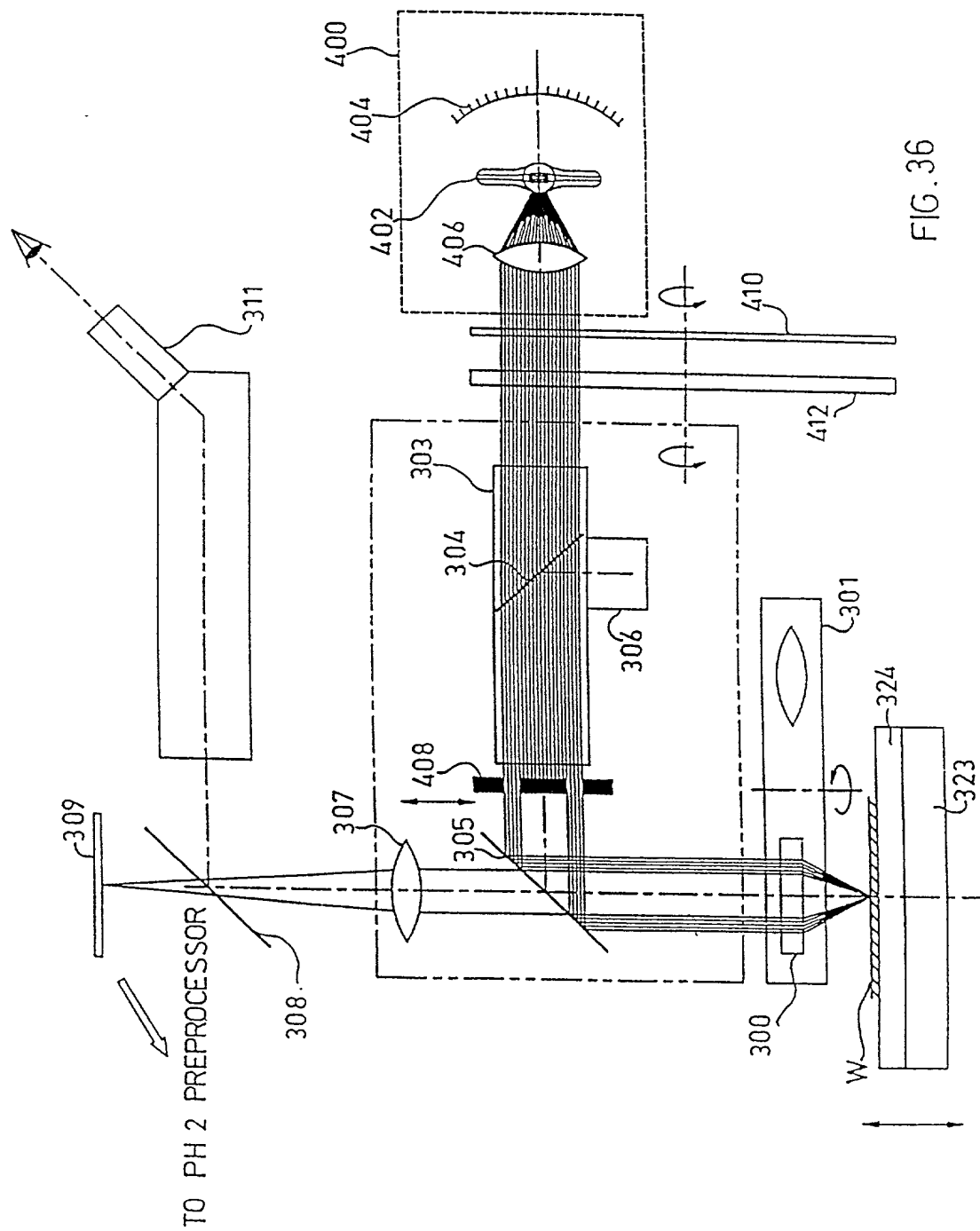
FIG 37











The diagram illustrates the architecture of the image processing system 9. It is divided into two main sections: PREPROCESSOR PHASE II and IMAGE PROCESSOR PHASE II.

**PREPROCESSOR PHASE II (340):** This section receives inputs from the CCD VID. (9) and CCD CONTR. (320). It contains a PRE AMP. block and a CCD CONTR. block. The output of the PRE AMP. is sent to the DIG. block in the next phase. The CCD CONTR. block also receives input from the FOCUS WHEEL and sends control signals to the DIG. block and the MEM. BUF. block.

**IMAGE PROCESSOR PHASE II:** This section contains the following components and connections:

- DIG. (321):** Receives input from the PRE AMP. and the CCD CONTR. block. Its output goes to the MEM. BUF. block.
- MEM. BUF. (322):** Receives input from the DIG. block and sends data to the DIGITAL SIGNAL PROCESSOR (323).
- DIGITAL SIGNAL PROCESSOR (323):** This block contains a COMP. (327) and a CLASS. (328) sub-block. It receives data from the MEM. BUF. and sends control signals to the SW. CONTR. block and the HARDWARE ACC. block.
- SW. CONTR. (324):** Receives input from the DIGITAL SIGNAL PROCESSOR and sends control signals to the MEM. BUF. and the CLASS. block.
- HARDWARE ACC. (329):** Receives input from the DIGITAL SIGNAL PROCESSOR and sends data to the CLASS. block.
- MAIN CONTR. (328):** Receives input from the CLASS. block and sends control signals to the SW. CONTR. block and the HARDWARE ACC. block.

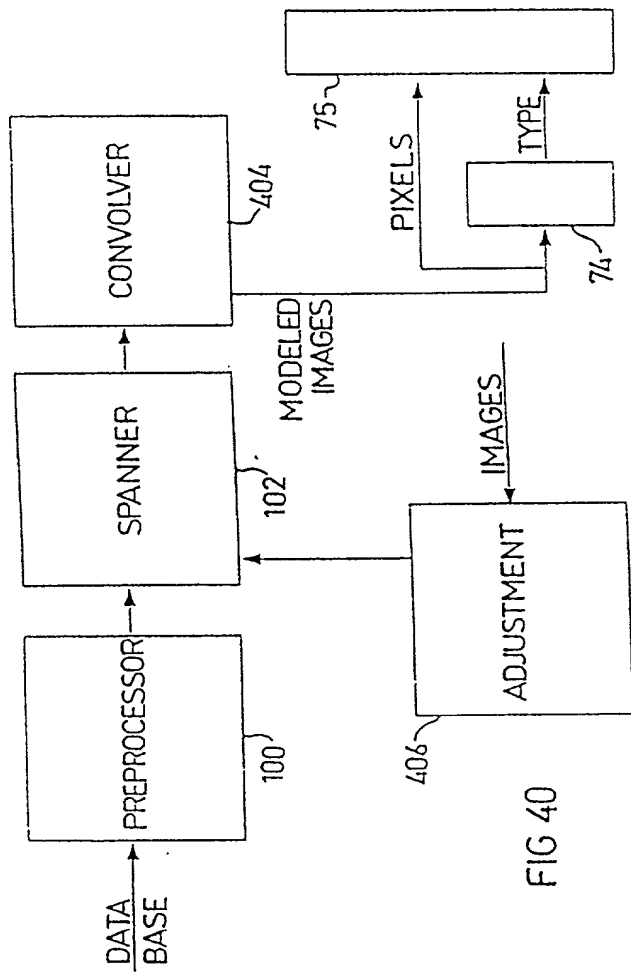


FIG 40

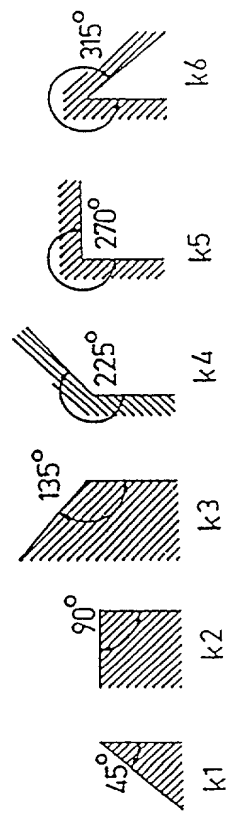
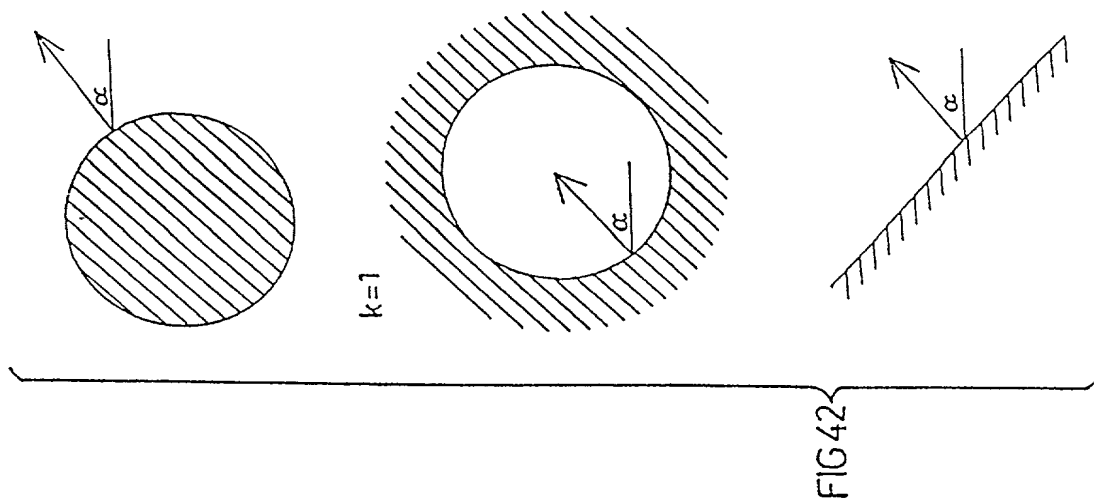
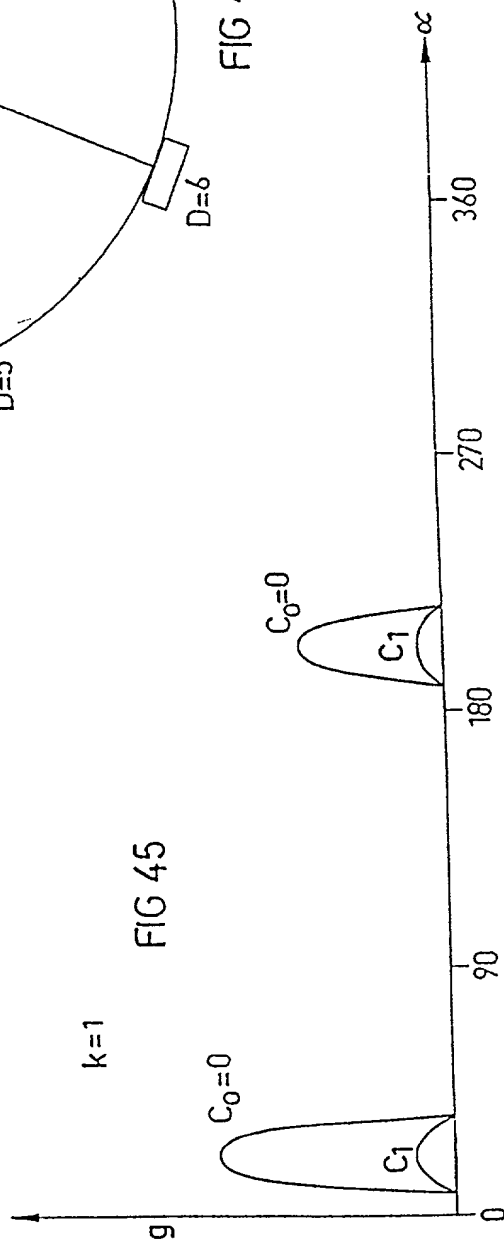
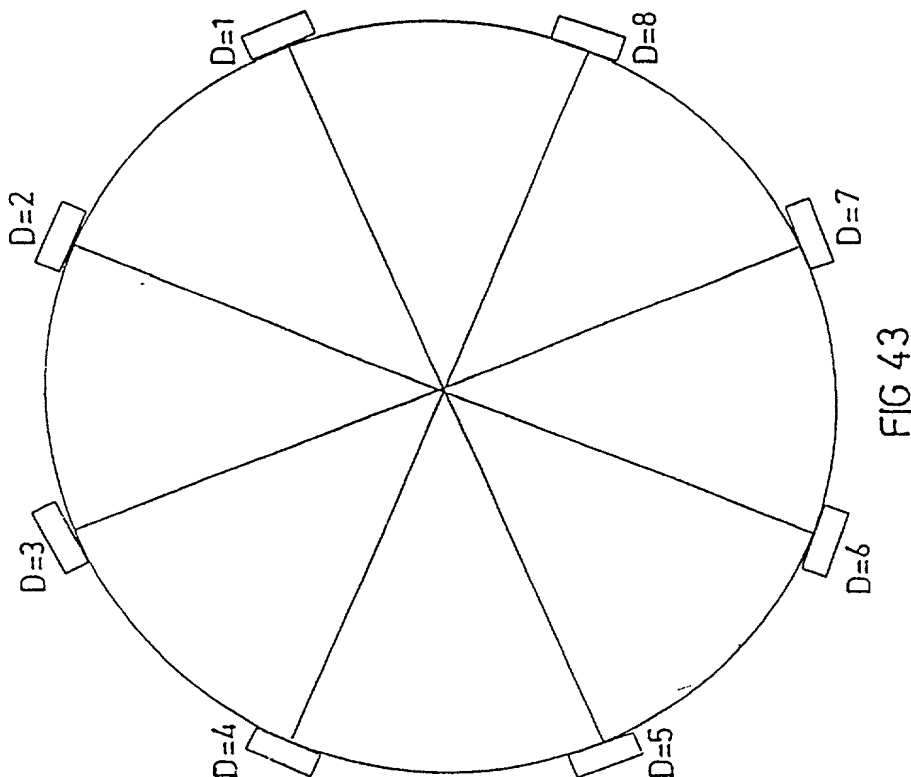
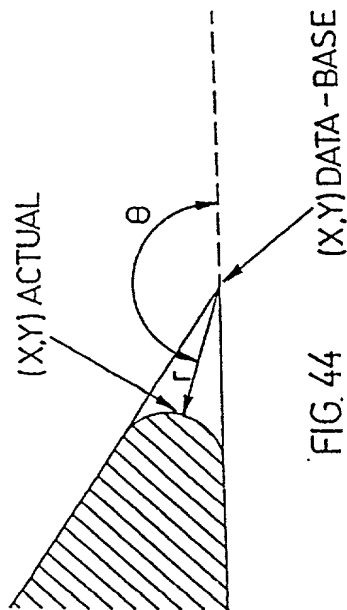
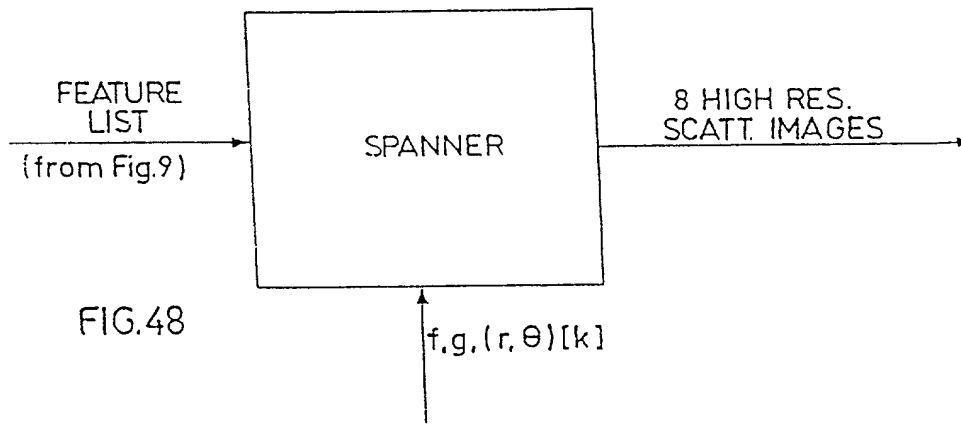
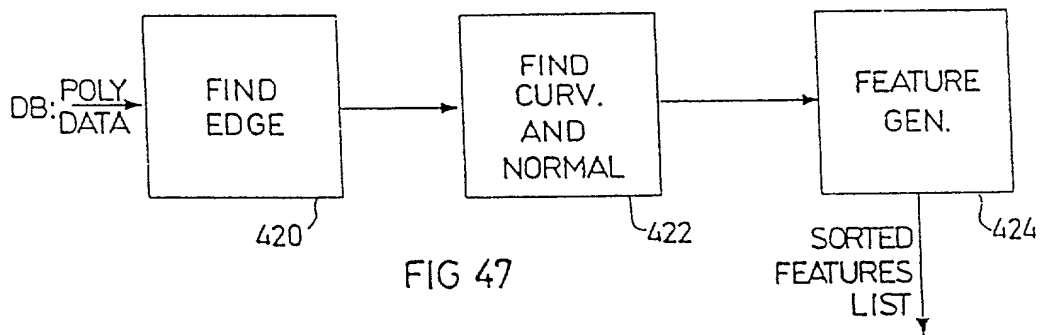
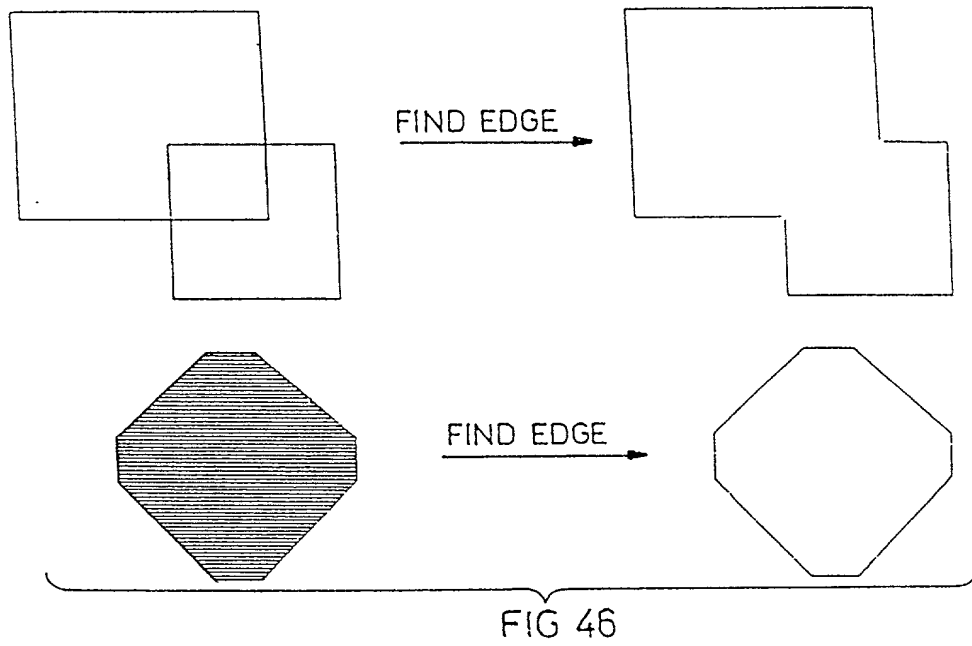


FIG. 41







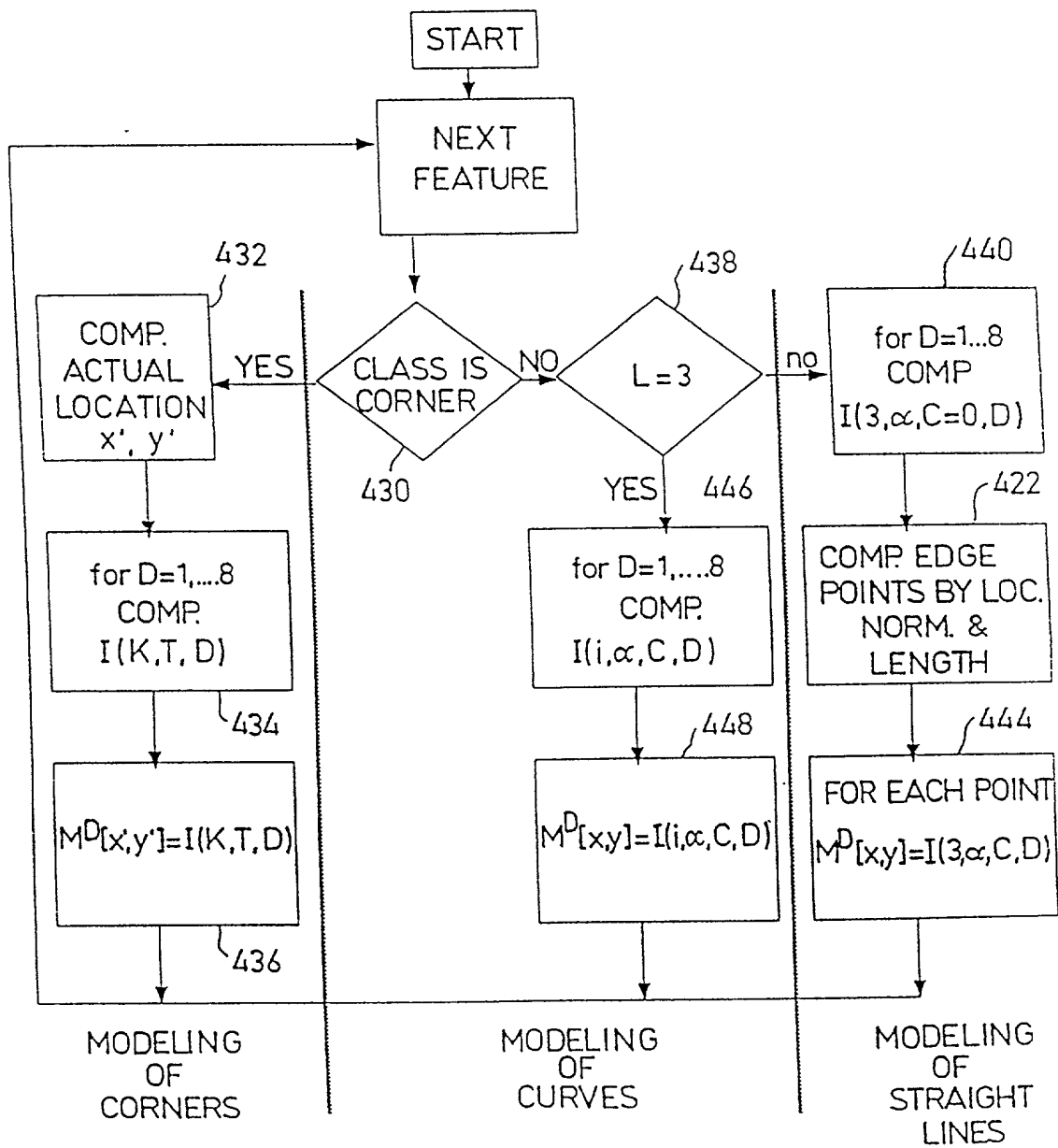


FIG 49